

PCB Number: 16544-1

ECO# number :

BOM Configuration

(A):Summit+Bristol

(S):CPU-Summit 65W

(B):CPU-Bristol 35W

(E):Ellesmere

(R):Unmount

(G):GPU

(U):UMA

(D):Debug used

(T):Touch

(L):GPU-Baffin G1-80 50W

(H):GPU-Ellesmere E1-90 110W

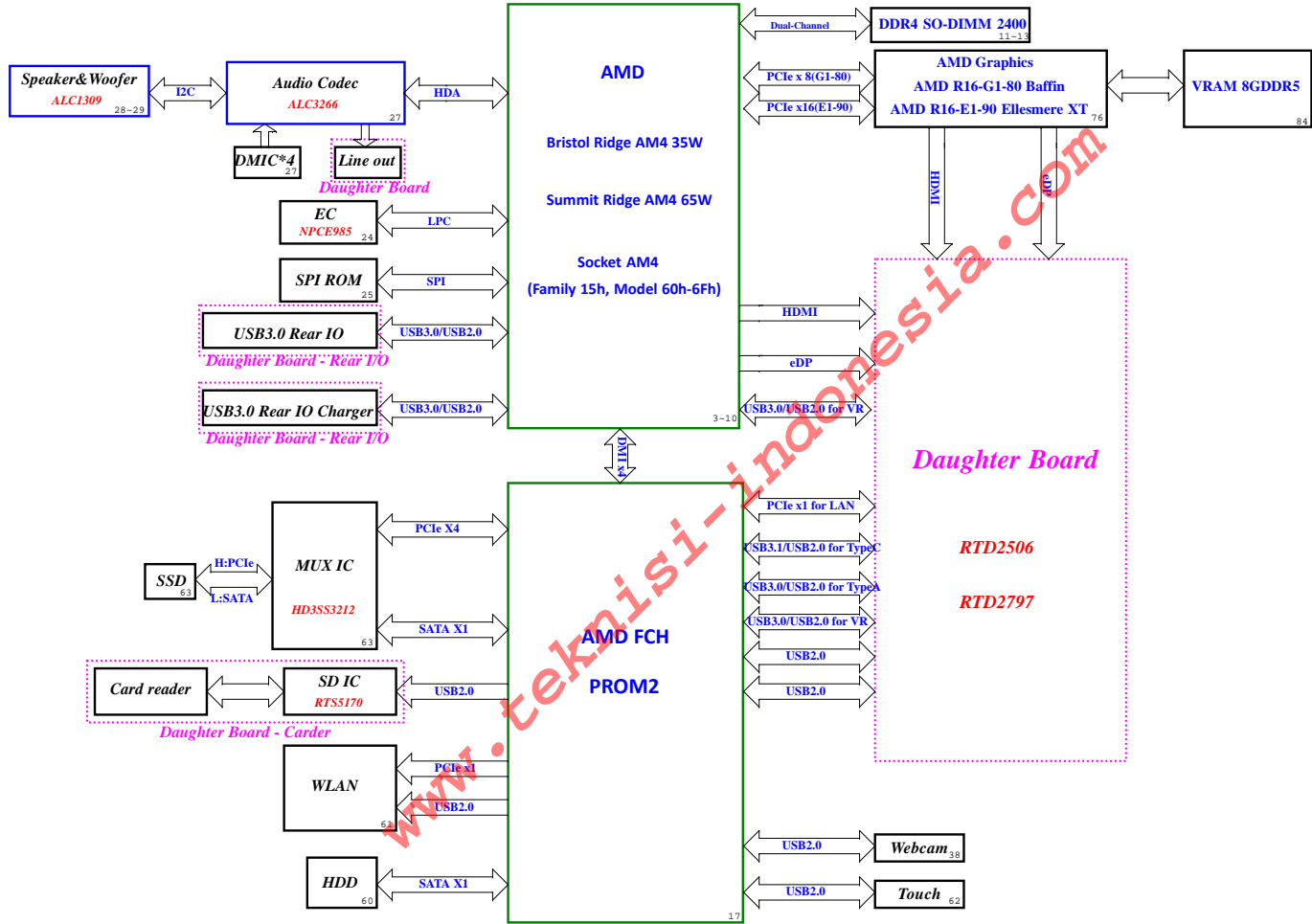
(Z):Type 3

PAGE	TITLE	Quantity
01	Cover Page	
02	Block Diagram	
03	AM4 PCIE I/F	
04	AM4 MEM DDR4	
05	AM4_DISPLAY/)/SVI2/JTAG	
06	AM4 ACPI/SD/GPIO/I2C/RTC	
07	AM4_CLK/USB/SPI/LPC	
08	AM4 Power	
09	AM4 VSS	
10	AM4 Power CAP	
11	Reserved	
12	DDR4_DIMMA0	
13	DDR4_DIMMB0	
14	Reserved	
15	Reserved	
16	STRAP_pins	
17	PROMONTORY PCIE/SATA	
18	PROMONTORY GPIO	
19	PROMONTORY USB/CLOCK	
20	PROMONTORY POWER	
21	PROMONTORY_Power_CAP	
22	Reserved	
23	Reserved	
24	EC_KBC_NPCE985PB1	
25	Flash ROM/RTC	
26	FAN CIRCUITS/HOLE	
27	CODEC_ALC3266	
28	AMP_ALC1309	
29	AMP_SUBWOOFER_ALC1309	
30	Reserved	
31	Reserved	
32	Reserved	
33	Reserved	
34	Side_I/O	
35	Rear_I/O_CN	
36	Rear_I/O_USB	
37	Reserved	
38	WEBCAM	
39	Reserved	
40	POWER SEQUENCE CTRL	
41	DCIN	
42	Run_PWR	
43	DDR4 POWER EN & SEQ	
44	IPCC_CY8C4124	
45	5V/3D3V(RT6575D)	
46	ISL62773A_CPUCORE(1/3)	
47	ISL62773A_CPUCORE(2/3)	
48	ISL62773A_CPUCORE(3/3)	
49	Reserved	
50	Reserved	
51	MEM_MEMVTT (RT8231)	
52	DCDC_VDDP(AOZ2262)/FCH_1D05	
53	DCDC_2D5V/1D8V/12V	
54	LDO_1D5V/0D775V	
55	Reserved	
56	Reserved	
57	Reserved	
58	Reserved	

PAGE	TITLE	Quantity
59	Reserved	
60	HDD	
61	M.2_(WLAN)_Key_A	
62	TOUCH	
63	M.2_(SSD)_Key_M	
64	LED BOARD/POWER BUTTON	
65	Reserved	
66	Reserved	
67	Reserved	
68	Debug port	
69	Reserved	
70	Reserved	
71	Reserved	
72	Reserved	
73	Reserved	
74	Reserved	
75	Reserved	
76	GPU_PCIE	
77	GPU_Main	
78	GPU_CLK	
79	GPU_Thermal & BACO & CTF	
80	GPU_GND	
81	POWER	
82	MEM_CH_AB	
83	MEM_CH_CD	
84	GDDR5_VRAM_BD	
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87	IO_Port	
88	GPU_3D3V_VGA	
89	GPU_CORE(1/2)	
90	GPU_CORE(2/2)	
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93	Reserved	
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98	Reserved	
99	099_HDT	
100	Reserved	
101	stack up	
102	Power sequence	
103	Power Block Diagram	
104	Power seq. Block Diagram	
105	Clock MAP	
106	RESET Flow Chart	
107	Reserved	

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SYSTEM DC/DC		
RT6575DQW-GP		45
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SYSTEM DC/DC		
RT6575DQW		45
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DCBATOUT	3D3V_S5	
DCBATOUT	3D3V_S0	
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APL5930KAI-TRG-1-GP54		
INPUTS	OUTPUTS	
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SYSTEM_1D05V_PCH_S5		
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SYSTEM_1D2V_MEM_S3		
RT8231AQW-GP		51
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SYSTEM_12V_S0		
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SYSTEM_1V_VDDCR_CPU		
1S62773AHR2-T-GP		47
INPUTS	OUTPUTS	
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SYSTEM_1V_VDDCR_CPU		
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DCBATOUT	1V_VDDCI_VGA	
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INPUTS	OUTPUTS	
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AOZ2262QI-10-GP-U		91
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DCBATOUT	1D35V_MEM_VGA	
PCB LAYER		
L1:TOP		
L2:GND		
L3:SINGLE/POWER		
L4:SINGLE/POWER		
L5:GND		
L6:SINGLE/POWER		
L7:GND		

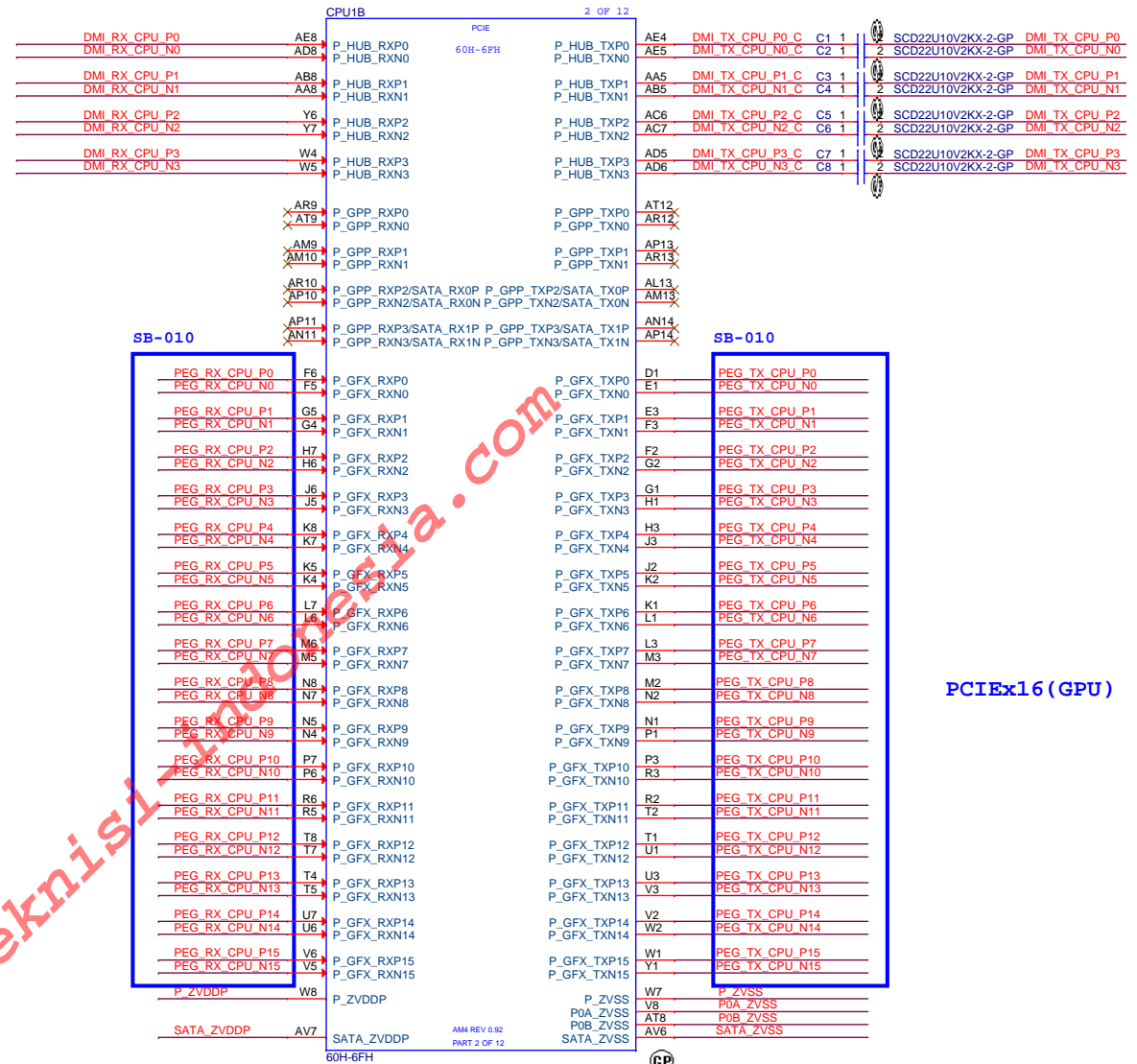
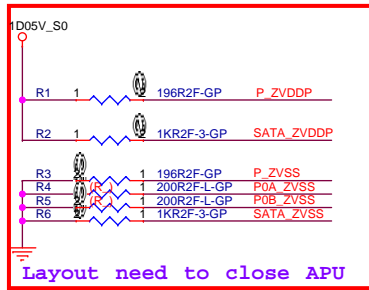
System switches		
INPUTS	OUTPUTS	
1D8V_S5	VDDP_S5(0.9V)	52
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1D8V_S5	0D775V_S5	54
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5V_S5	5V_S0	42
3D3V_S5	3D3V_S0	42
3D3V_S5	2D5V_PCH_S0	53
1D05V_PCH_S5	1D05V_PCH_S0_L	42
1D05V_S5	1D05V_S0	42
1D8V_S5	1D8V_S0	42
3D3V_S0	3D3V_VGA	88
3D3V_S5	1D8V_VGA	91

PCIE*16 GPU

76 PEG_TX_CPU_P[15:0] <<< <<<
76 PEG_TX_CPU_N[15:0] <<< <<<
76 PEG_RX_CPU_P[15:0] <<< <<<
76 PEG_RX_CPU_N[15:0] <<< <<<

DMI

17 DMI_RX_CPU_P[0..3] <<< <<<
17 DMI_RX_CPU_N[0..3] <<< <<<
17 DMI_TX_CPU_P[0..3] <<< <<<
17 DMI_TX_CPU_N[0..3] <<< <<<



2.12.4.5.1 Lane Reversal

Normally, the lanes of each port are physically numbered from n-1 to 0 where n is the number of lanes assigned to the port. Physical lane numbering can be reversed according to the following methods:

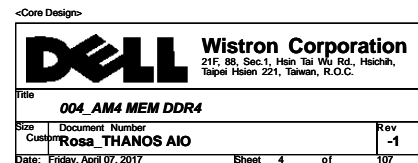
- To reverse the physical lane numbering for a specific port, program D[3:2]F[5:1]xE4_xC1[StrapReverse-Lanes] = 1.
- To reverse the physical lane numbering for all ports in the GPP or GFX interfaces, program D0F0xE4_x014[1:0]_00C0[StrapReverseAll] = 1.

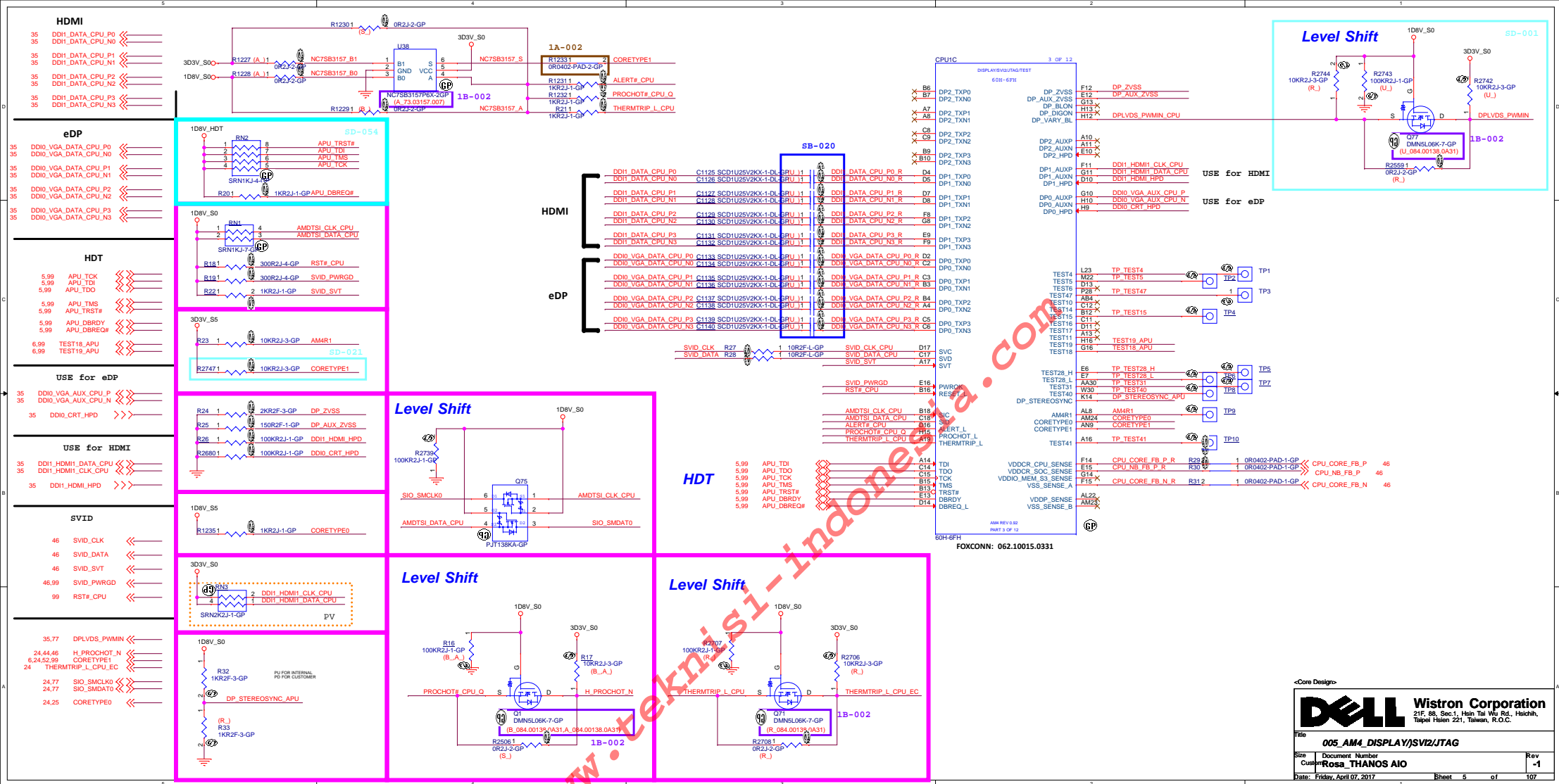
Note that logical port numbering is established during link training regardless of the physical lane numbering.

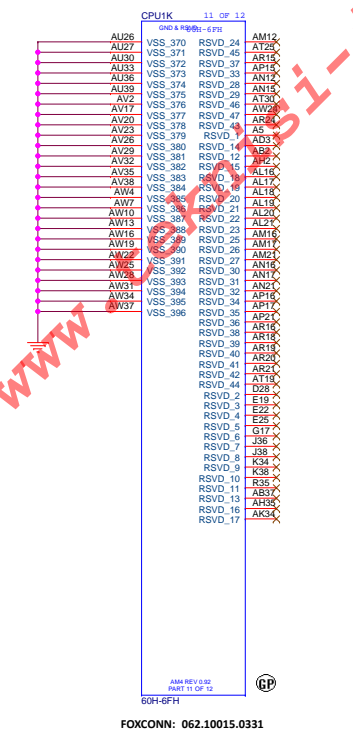
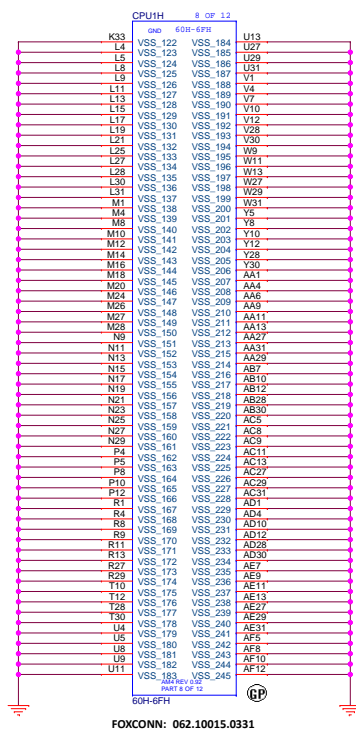
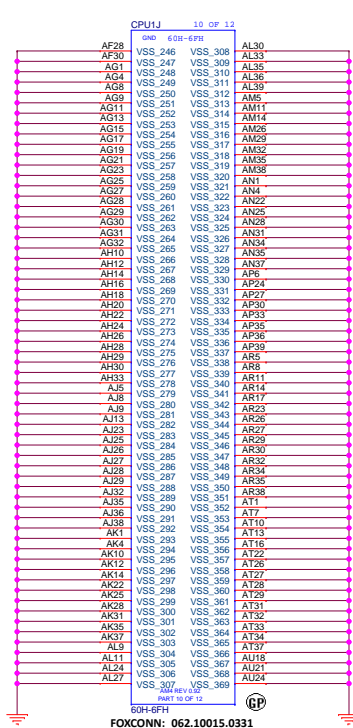
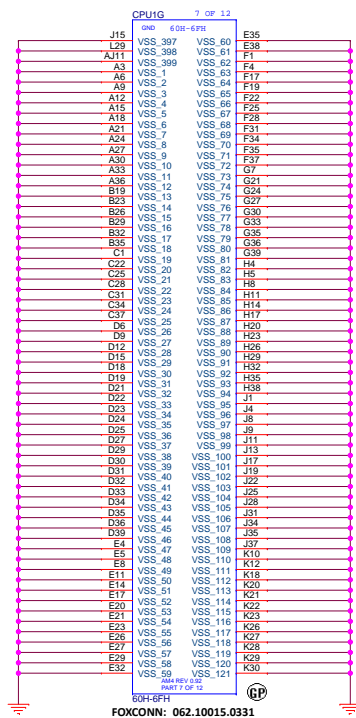
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003_AM4_PCIE_I/F			
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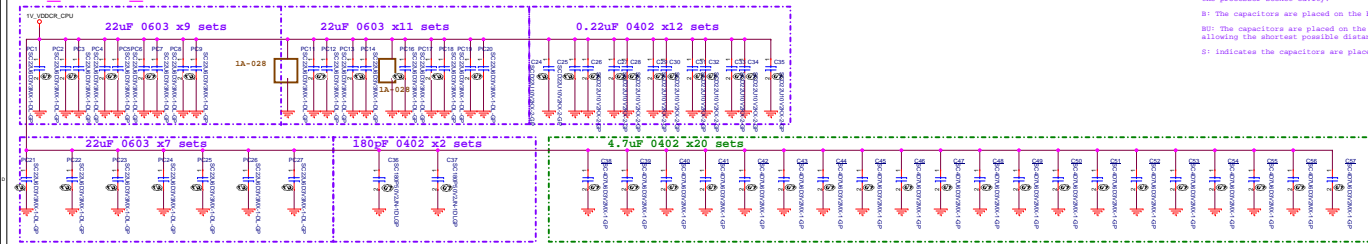
DIMM2





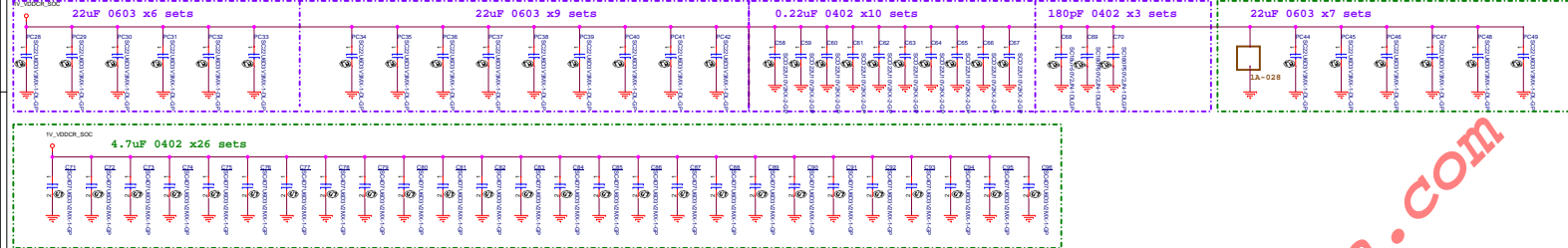


1V_VDDCR_CPU CRB 22uF*27 4.7uF*20 0.22uF*12 180pF*2 Checklist 22uF*27 4.7uF*20 0.22uF*12 180pF*2

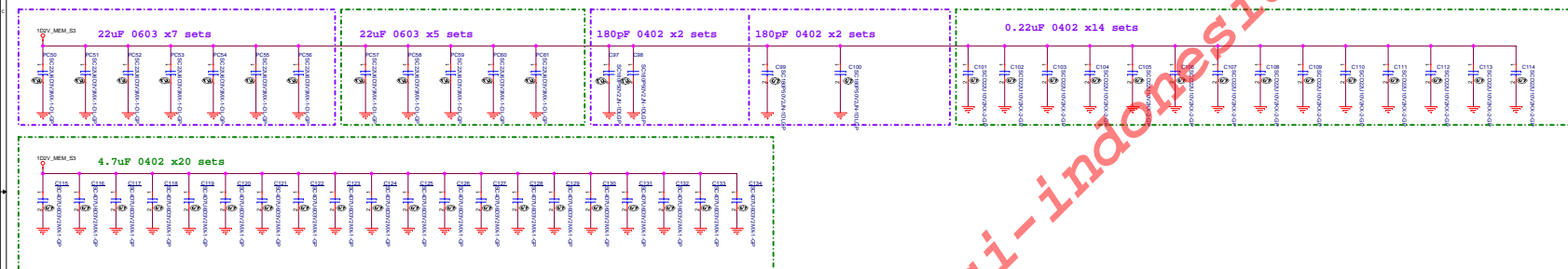


T1: The capacitors are placed on the top side (on the same side as the processor) of the board inside the processor cavity.
S1: The capacitors are placed on the bottom side of the board.
S2: The capacitors are placed on the bottom side of the board, under the processor socket, thereby allowing the shortest possible distance from the power plane.
S3: Indicates the capacitors are placed on the VDDIO_MEM_S3 plane split.

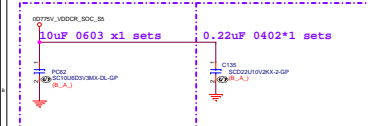
1V_VDDCR_SOC CRB 22uF*22 4.7uF*26 0.22uF*10 180pF*3 Checklist 22uF*22 4.7uF*26 0.22uF*10 180pF*3



1D2V_MEM_S3 CRB 22uF*12 4.7uF*20 0.22uF*14 180pF*4 Checklist 22uF*12 4.7uF*20 0.22uF*14 180pF*4

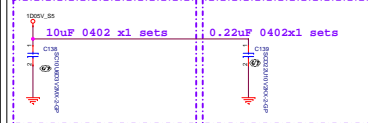


0D775V_VDDCR_SOC_S5



CRB 10uF*1 0.22uF*1
Checklist 10uF*1 0.22uF*1

1D05V_S5 CRB 10uF*1 0.22uF*1 Checklist 10uF*1 0.22uF*1



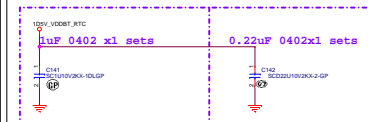
1D05V_S0

CRB 22uF*4 10uF*2 0.22uF*1 1000pF*1 180pF*3
Checklist 22uF*2 10uF*1 0.22uF*1



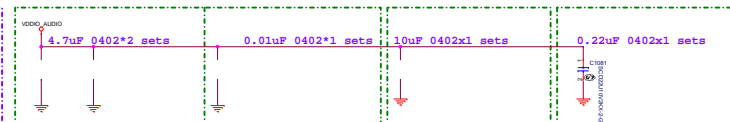
1D5V_VDDBT_RTC

CRB 1uF*1 0.22uF*1
Checklist 1uF*1 0.22uF*1



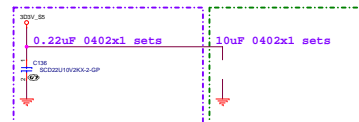
1D5V_S5 (VDDIO_AUDIO)

CRB 4.7uF*2 0.01uF*1 10uF*1 0.22uF*1
Checklist 0.22uF*1



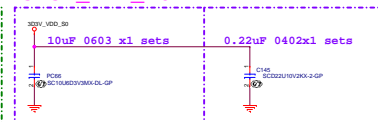
3D3V_S5

CRB 0.22uF*1 10uF*1
Checklist 0.22uF*1

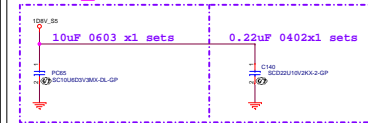


3D3V_VDD_S0

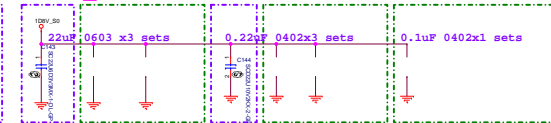
CRB 10uF*1 0.22uF*1
Checklist 10uF*1 0.22uF*1



1D8V_S5 CRB 10uF*1 0.22uF*1 Checklist 10uF*1 0.22uF*1




1D8V_S0 CRB 22uF*3 0.22uF*3 0.1uF*1 Checklist 22uF*1 0.22uF*1



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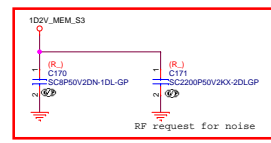
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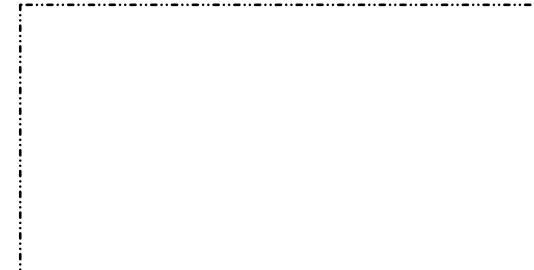
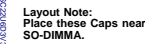
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Note:
SA0_DIMM1 = 0, SA1_DIMM1 =
SO-DIMMA SPD Address is 0xA
SO-DIMMA TS Address is 0x30

Note:
SA0_DIMM1 = 0, SA1_DIMM1 =
SO-DIMMA SPD Address is 0xA
SO-DIMMA TS Address is 0x30




SMBus 0			
Device	8-bit Address(hex)		
DIMM A0	Read Address:0x02	SA1=0:SA0=0	
DIMM A1	Write Address:0x02	SA1=0:SA0=0	
DIMM B0	Write Address:0x02	SA1=1:SA0=0	
DIMM B1	Read Address:0x02	SA1=1:SA0=0	
1	0	0	SA1 SA0

Note:0' 3~7 bit as default

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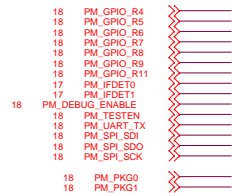
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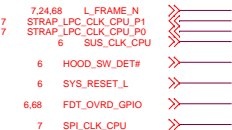
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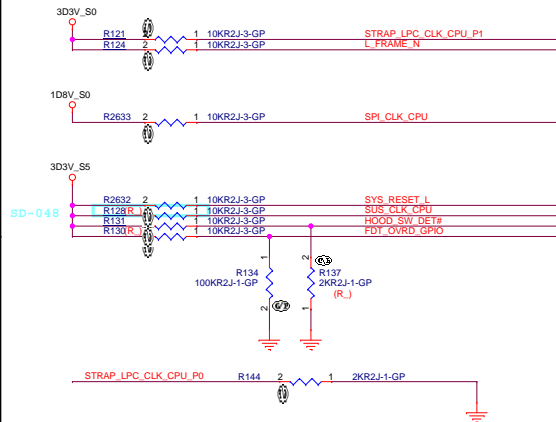
PCH STRAP



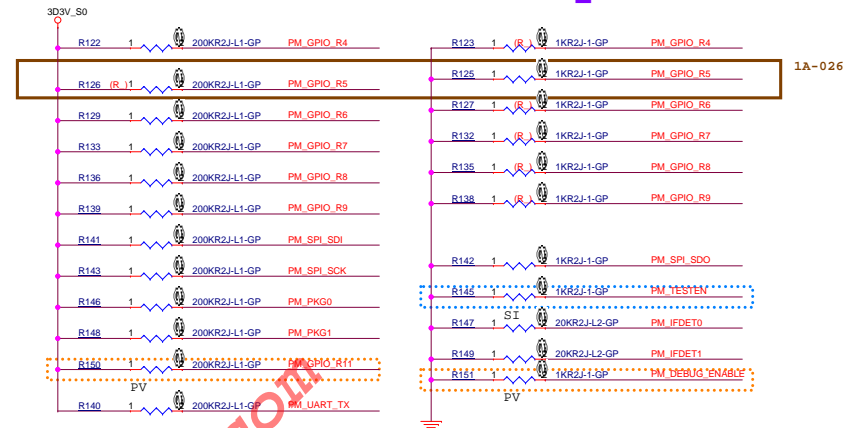
CPU STRAP



AM4 FPU HW Strap



PROM HW Strap



Strap Name	Signal Name	Strap Type	Default Value	Bit Value	Description	Net name	Default Value
CLKGEN AM4 Type0, Type 2, and Type 3 processors	LPCCLK1	Strap II	1	0	Reserved	STRAP_LPC_CLK_CPU_P1	1
	SPI_CLK			1	Configured for internal clock-generator LPCCLK1 = 10 kΩ (± 5%) pull-up resistor to VDD_18	SPI_CLK_CPU	1
ShortReset AM4 Type 0, Type 2, and Type 3 processors	SYS_RESET_L	Strap I	1	0	Reserved	SYS_RESET_L	1
				1	Normal powerup/reset timing 10 kΩ (± 5%) pull-up resistor to VDD_33_S5		
ROMTYPE AM4 Type 0 and Type 2 processors only	LFRAME_L	Strap II	1	0	LPC ROM	L_FRAME_N	1
				1	SPI ROM 10 kΩ (± 5%) pull-up resistor to VDD_33		
BOOTFAILTIM ER AM4 Type 0 processor only	LPCCLK0	Strap II	0	0	Boot Fail Timer Disabled	STRAP_LPC_CLK_CPU_P0	0
				1	Boot Fail Timer Enabled 10 kΩ (± 5%) pull-up resistor to VDD_33		
RTC Coin Battery AM4 Type 0 processor only	RTCCLK	Strap I	1	0	RTC Coin Battery is not implemented	SUS_CLK_CPU	1
				1	RTC Coin Battery is implemented 10 kΩ (± 5%) pull-up resistor to VDD_33_S5		
Alternate Reset AM4 Type 0 processor only	AGPIO3	Strap I	1	0	Traditional Reset logic	HOOD_SW_DET#	1
				1	Enhanced Reset logic for faster resume from S5 10 kΩ (± 5%) pull-up resistor to VDD_33_S5		

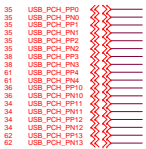
Signal Name	Function	Net name	Default Value
GPIO_R[4]	1: GPP clock source from APU_CLKP/N; 0: GPP clock source from Crystal, also enables GPIO_R8	PM_GPIO_R4	1
GPIO_R[5]	1: USB3 SSC disable 0: USB3 SSC enable	PM_GPIO_R5	1
GPIO_R[6]	1: SATA SSC disable 0: SATA SSC enable	PM_GPIO_R6	1
GPIO_R[7]	1: SATA Express SSC disable 0: SATA Express SSC enable	PM_GPIO_R7	1
GPIO_R[8]	1: GPP SSC disable 0: GPP SSC enable	PM_GPIO_R8	1
GPIO_R[9]	Whole Chip SSC (Spread Spectrum Clock) 1: Disable (Default) 0: Enable	PM_GPIO_R9	1
GPIO_R[11]	1: GPP clock output enabled 0: GPP clock output disabled	PM_GPIO_R11	1
IFDET0	SATA Express port1 1: PCIe mode 0: SATA mode	PM_IFDET0	0
IFDET1	SATA Express port0 1: PCIe mode 0: SATA mode	PM_IFDET1	0
DEBUG_ENABLE	1: Debug mode 0: Function mode	PM_DEBUG_ENABLE	0
TESTEN	Test mode enable 1: Test mode 0: Function mode	PM_TESTEN	0
UART_TX (GPP_G1_SET1) SPL_SDI (GPP_G1_SET0)	GPP Group1 11: 1 PCIe x4; 10: 1 PCIe x2+2 PCIe x1; 01: 4 PCIe x1; 00: Reserved	PM_UART_TX PM_SPL_SDI	1 1
SPL_SDO (GPP_G0_SET1) SPL_SCK (GPP_G0_SET0)	GPP Group0 11: 1 PCIe x4; 10: 1 PCIe x2+2 PCIe x1; 01: 4 PCIe x1; 00: Reserved	PM_SPL_SDO PM_SPL_SCK	0 1

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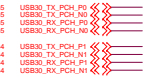
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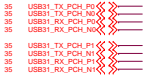
USB2.0



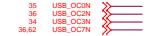
USB3.0



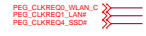
Type-C(USB3.1)



USB OC



CLKREQ



CLOCK



BUS Model	USB			
	3.1 Gen2 10 Gbps	3.1 Gen1 5 Gbps	2.0	Debug Port
PROM4	USB_SSP Port0~1	USB_SS Port 0~5	USB_HSD Port0~13	USB_SSP Port0
PROM2	USB_SSP Port0~1	USB_SS Port 0~1	USB_HSD Port0~5 USB_HSD Port10~13	USB_SSP Port0
PROM1	USB_SSP Port0	USB_SS Port0 USB_SSP Port1	USB_HSD Port0~5 USB_HSD Port10, 12~13	USB_SSP Port0

USB3.1	USB2.0	USB_OC
USB_SSP_TX/RXP/N[0]	USB_HSDP/N[5]	USB_OC0N
USB_SSP_TX/RXP/N[1]	USB_HSDP/N[0]	USB_OC1N
USB3.0	USB2.0	USB_OC
USB_SS_TX/RXP/N[0]	USB_HSDP/N[10]	USB_OC2N
USB_SS_TX/RXP/N[1]	USB_HSDP/N[11]	USB_OC3N
USB_SS_TX/RXP/N[2]	USB_HSDP/N[6]	USB_OC4N
USB_SS_TX/RXP/N[3]	USB_HSDP/N[7]	USB_OC5N
USB_SS_TX/RXP/N[4]	USB_HSDP/N[8]	USB_OC6N
USB_SS_TX/RXP/N[5]	USB_HSDP/N[9]	USB_OC7N
USB_HSDP/N[1]	USB_OC7N	
USB_HSDP/N[2]	USB_OC7N	
USB_HSDP/N[3]	USB_OC7N	
USB_HSDP/N[4]	USB_OC7N	
USB_HSDP/N[12]	USB_OC7N	
USB_HSDP/N[13]	USB_OC7N	

USB 2.0 Table

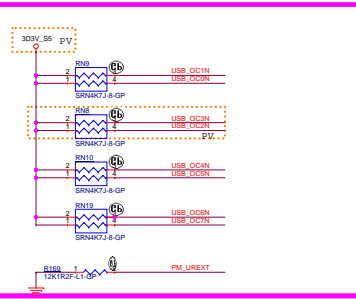
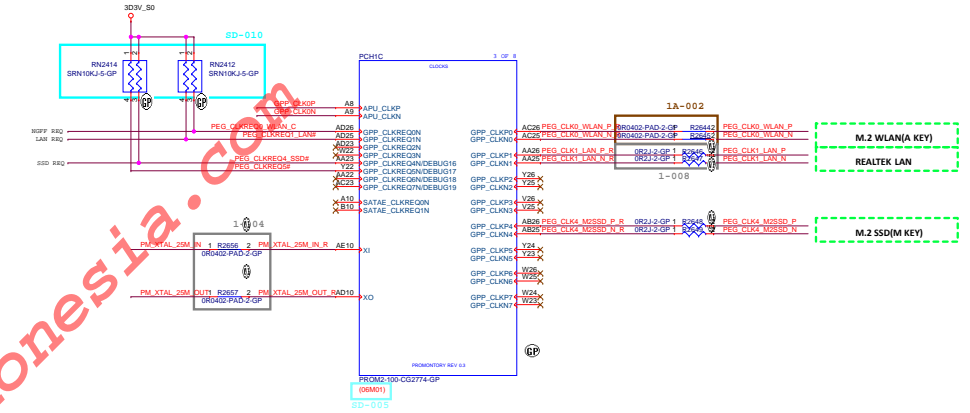
Pair	Device
0	Type-C
1~2	Rear IO USB 2.0
3	Webcam
4	Wireless+BT
10	Rear IO USB 3.0
11	Sido IO USB 3.0
12	Card Reader
13	Touch Panel

USB 3.0 Table

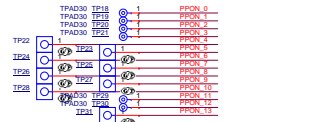
Pair	Device
0	Rear IO USB 3.0
1	Sido IO USB 3.0

USB 3.1 Table

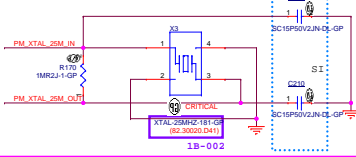
Pair	Device
0~2	Type-C



Test point

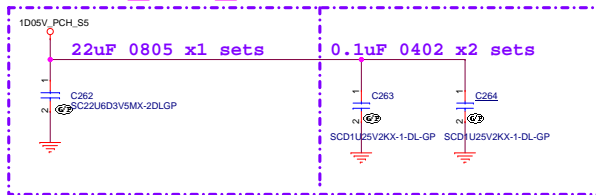


LAN XTAL



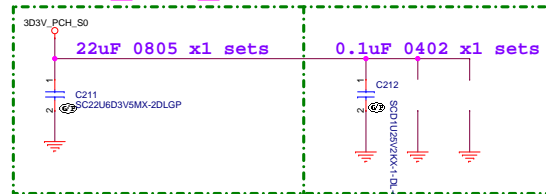
1D05V_PCH_S5

CRB 22uF*1 0.1uF*2
Checklist 22uF*1 0.1uF*2



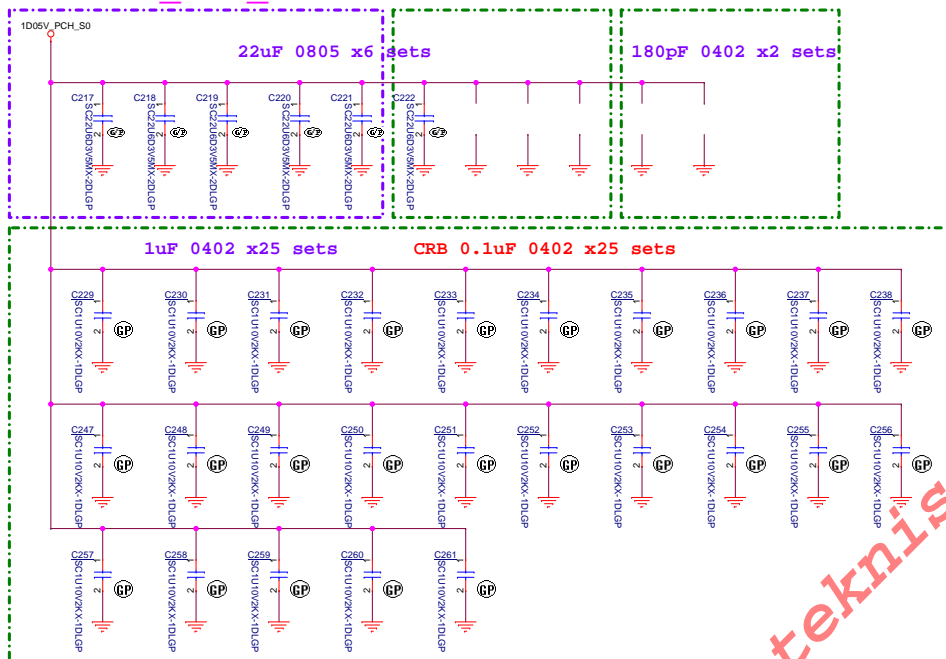
3D3V_PCH_S0

CRB 22uF*1 0.1uF*3
Checklist 22uF*1 0.1uF*1



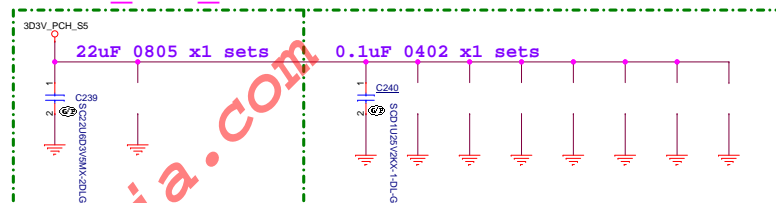
1D05V_PCH_S0

CRB 22uF*9 0.1uF*25 180pF*2
Checklist 22uF*6 0.1uF*25



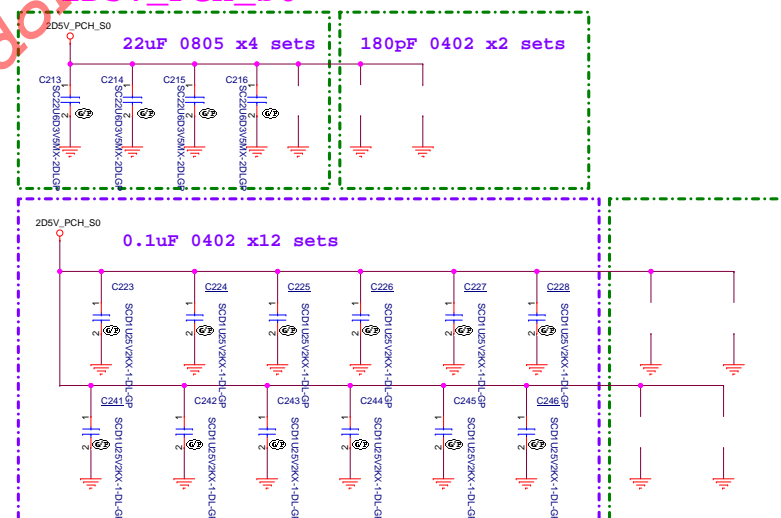
3D3V_PCH_S5

CRB 22uF*2 0.1uF*8
Checklist 22uF*1 0.1uF*1



2D5V_PCH_S0

CRB 22uF*5 0.1uF*16 180pF*2
Checklist 22uF*4 0.1uF*12



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021_PROMONTORY_Power_CAP

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022_(Reserved)

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023 (Reserved)

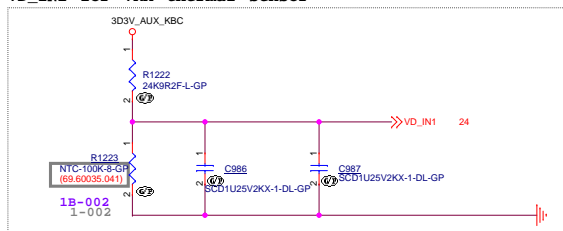
Size	Document Number	Rev
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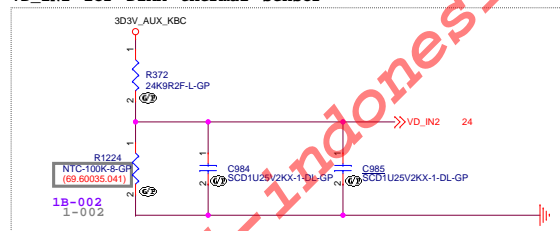
24 CPU_FAN_CTRL_SIO >>>
24 CPU_FAN_TACH_SIO <<<

[illegible]

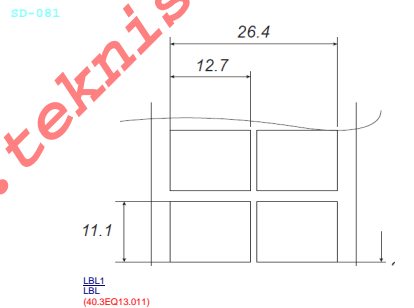
VD IN1 for VRM thermal sensor



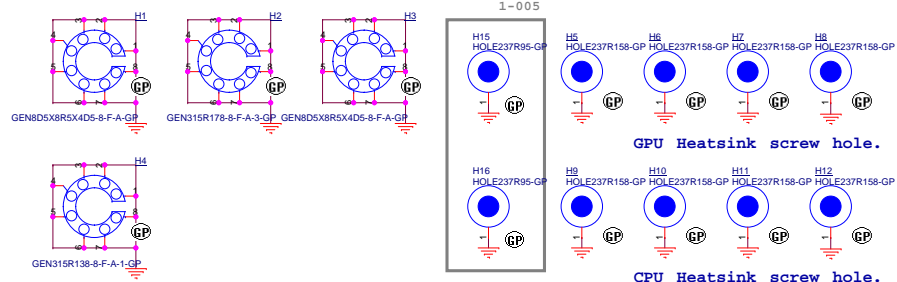
VD IN2 for DIMM thermal sensor



Technical drawing of a rectangular plate. Dimensions: width 37 ± 0.2 , height 31 ± 0.2 , and distance from top-left corner to center of hole 24 ± 0.2 . Hole diameter is $\varnothing 5.50$. A detail view (1) shows a cross-section of the plate with a hole, a spring, and a pin.



LBL1
LBL
(40.3EQ13.011)



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026_FAN CIRCUITS/HOLE

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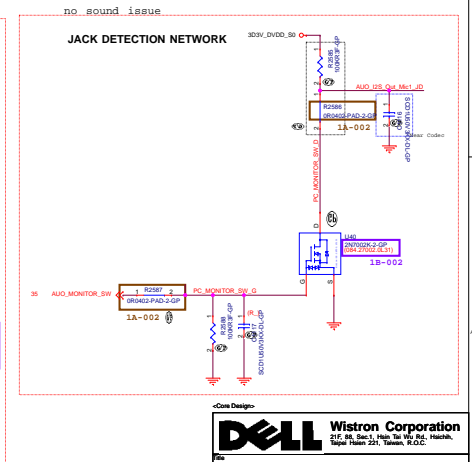
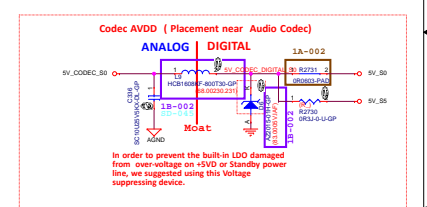
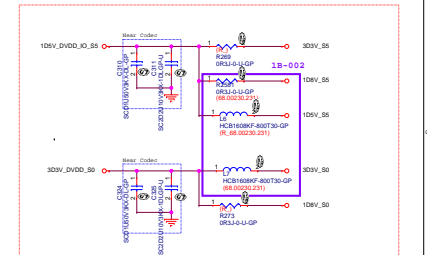
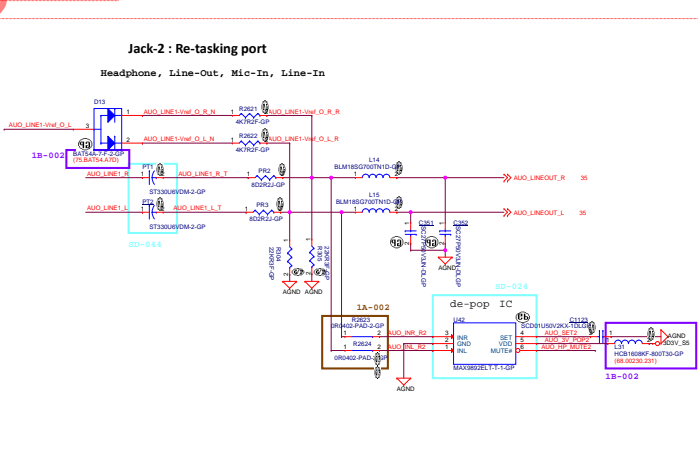
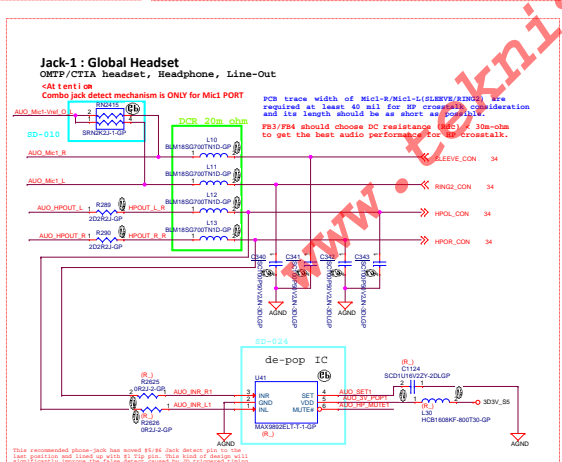
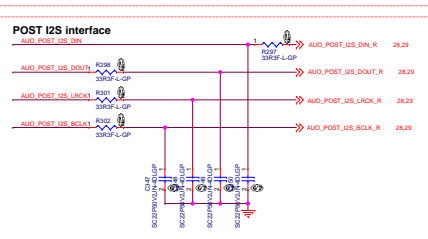
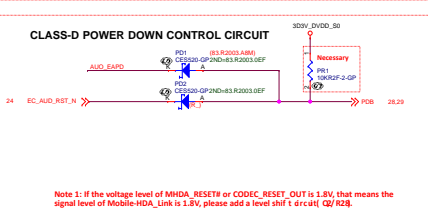
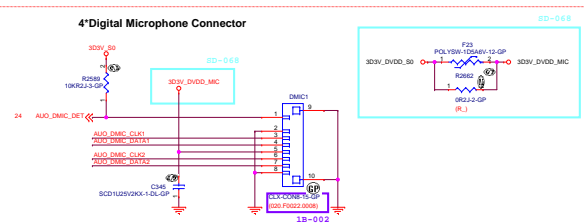
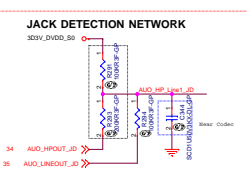
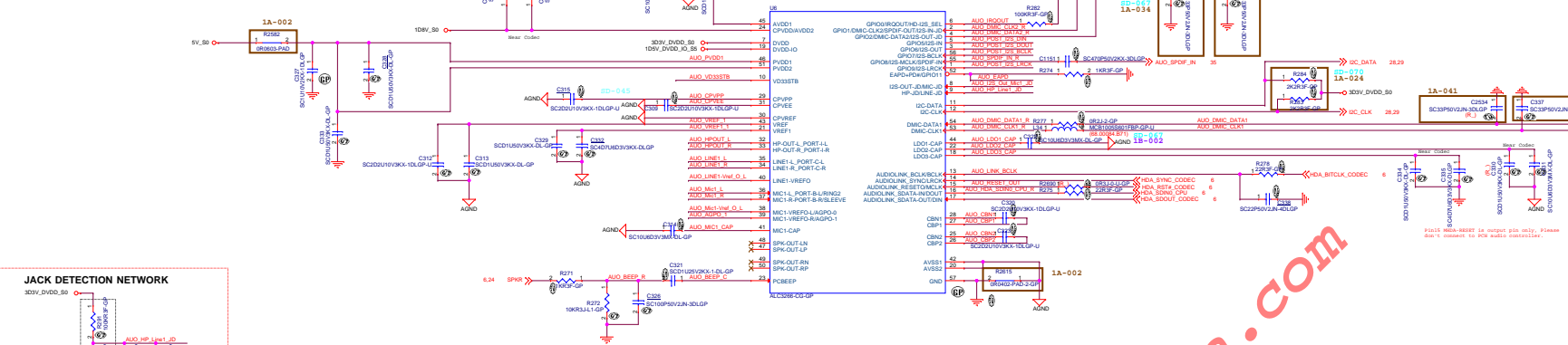
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Power	Pin	Function	Notes
1.8V	1	1.8V	1.8V
1.8V	2	1.8V	1.8V
1.8V	3	1.8V	1.8V
1.8V	4	1.8V	1.8V
1.8V	5	1.8V	1.8V
1.8V	6	1.8V	1.8V
1.8V	7	1.8V	1.8V
1.8V	8	1.8V	1.8V
1.8V	9	1.8V	1.8V
1.8V	10	1.8V	1.8V
1.8V	11	1.8V	1.8V
1.8V	12	1.8V	1.8V
1.8V	13	1.8V	1.8V
1.8V	14	1.8V	1.8V
1.8V	15	1.8V	1.8V
1.8V	16	1.8V	1.8V
1.8V	17	1.8V	1.8V
1.8V	18	1.8V	1.8V
1.8V	19	1.8V	1.8V
1.8V	20	1.8V	1.8V
1.8V	21	1.8V	1.8V
1.8V	22	1.8V	1.8V
1.8V	23	1.8V	1.8V
1.8V	24	1.8V	1.8V
1.8V	25	1.8V	1.8V
1.8V	26	1.8V	1.8V
1.8V	27	1.8V	1.8V
1.8V	28	1.8V	1.8V
1.8V	29	1.8V	1.8V
1.8V	30	1.8V	1.8V
1.8V	31	1.8V	1.8V
1.8V	32	1.8V	1.8V
1.8V	33	1.8V	1.8V
1.8V	34	1.8V	1.8V
1.8V	35	1.8V	1.8V
1.8V	36	1.8V	1.8V
1.8V	37	1.8V	1.8V
1.8V	38	1.8V	1.8V
1.8V	39	1.8V	1.8V
1.8V	40	1.8V	1.8V
1.8V	41	1.8V	1.8V
1.8V	42	1.8V	1.8V
1.8V	43	1.8V	1.8V
1.8V	44	1.8V	1.8V
1.8V	45	1.8V	1.8V
1.8V	46	1.8V	1.8V
1.8V	47	1.8V	1.8V
1.8V	48	1.8V	1.8V
1.8V	49	1.8V	1.8V
1.8V	50	1.8V	1.8V
1.8V	51	1.8V	1.8V
1.8V	52	1.8V	1.8V
1.8V	53	1.8V	1.8V
1.8V	54	1.8V	1.8V
1.8V	55	1.8V	1.8V
1.8V	56	1.8V	1.8V
1.8V	57	1.8V	1.8V
1.8V	58	1.8V	1.8V
1.8V	59	1.8V	1.8V
1.8V	60	1.8V	1.8V
1.8V	61	1.8V	1.8V
1.8V	62	1.8V	1.8V
1.8V	63	1.8V	1.8V
1.8V	64	1.8V	1.8V
1.8V	65	1.8V	1.8V
1.8V	66	1.8V	1.8V
1.8V	67	1.8V	1.8V
1.8V	68	1.8V	1.8V
1.8V	69	1.8V	1.8V
1.8V	70	1.8V	1.8V
1.8V	71	1.8V	1.8V
1.8V	72	1.8V	1.8V
1.8V	73	1.8V	1.8V
1.8V	74	1.8V	1.8V
1.8V	75	1.8V	1.8V
1.8V	76	1.8V	1.8V
1.8V	77	1.8V	1.8V
1.8V	78	1.8V	1.8V
1.8V	79	1.8V	1.8V
1.8V	80	1.8V	1.8V
1.8V	81	1.8V	1.8V
1.8V	82	1.8V	1.8V
1.8V	83	1.8V	1.8V
1.8V	84	1.8V	1.8V
1.8V	85	1.8V	1.8V
1.8V	86	1.8V	1.8V
1.8V	87	1.8V	1.8V
1.8V	88	1.8V	1.8V
1.8V	89	1.8V	1.8V
1.8V	90	1.8V	1.8V
1.8V	91	1.8V	1.8V
1.8V	92	1.8V	1.8V
1.8V	93	1.8V	1.8V
1.8V	94	1.8V	1.8V
1.8V	95	1.8V	1.8V
1.8V	96	1.8V	1.8V
1.8V	97	1.8V	1.8V
1.8V	98	1.8V	1.8V
1.8V	99	1.8V	1.8V
1.8V	100	1.8V	1.8V

1.8V power rail should be supplied by linear regulator, not switching regulator. if switching regulator is unavoidable, Please make sure that switching frequency operates at out of band (over 20KHz).



reference from Realtek

Table 15. Amp Output Terminal and Output Signal Mapping

Channel	Amp Output Terminal	Output Signal Mapping
1 Channel	Output	1 Channel Positive Output
2 Channel	Output	2 Channel Positive Output
3 Channel	Output	3 Channel Positive Output
4 Channel	Output	4 Channel Positive Output

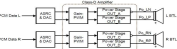
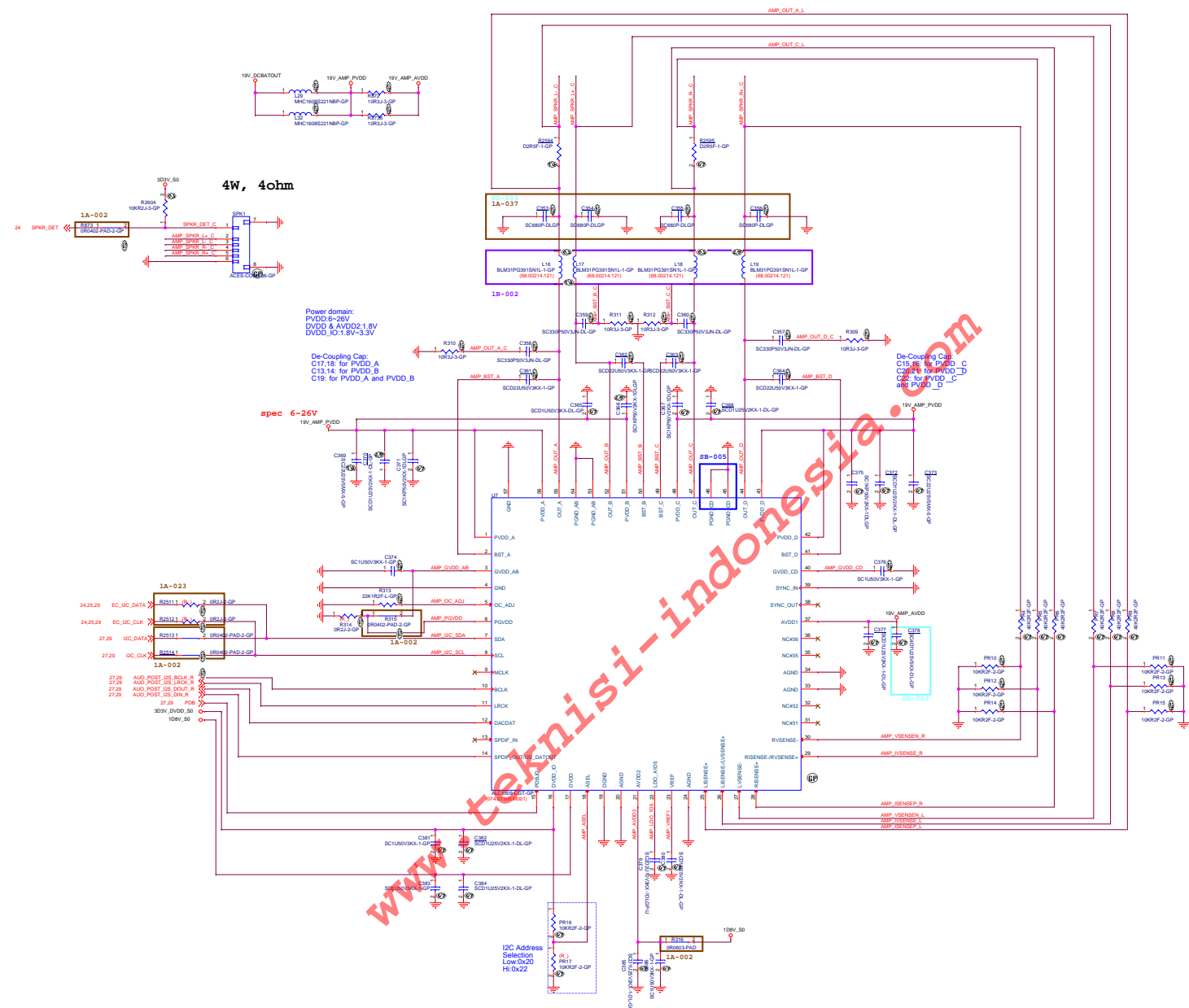



Figure 15. BTL Mode & Speaker Connection



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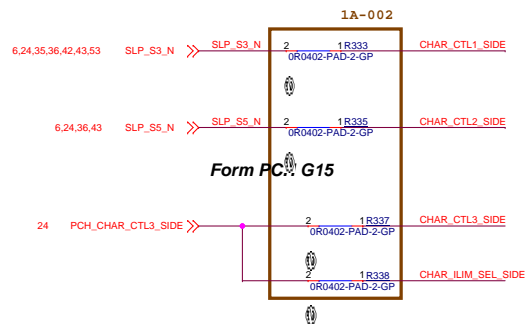
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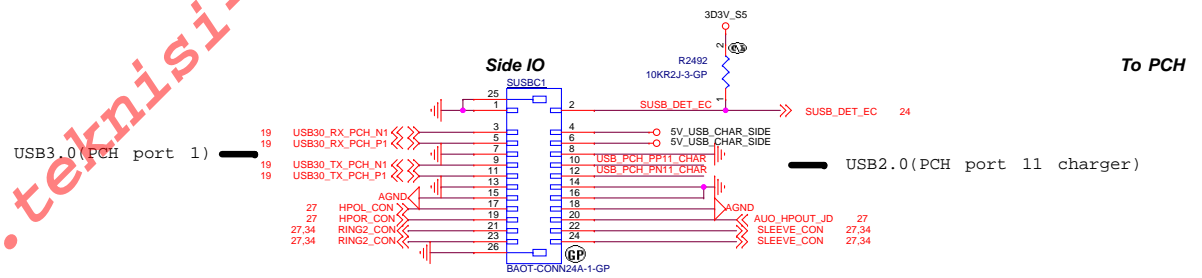
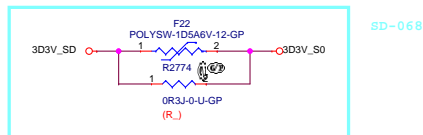
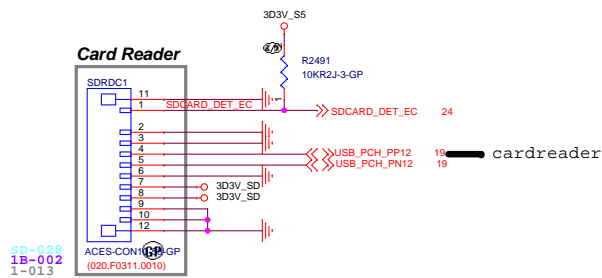
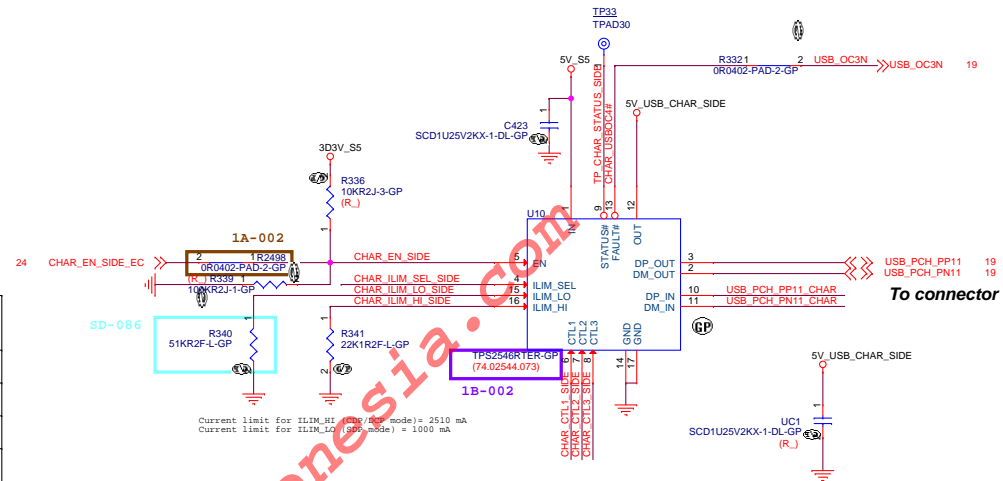
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Side I/O Charger

Charger IC - TI TPS2546

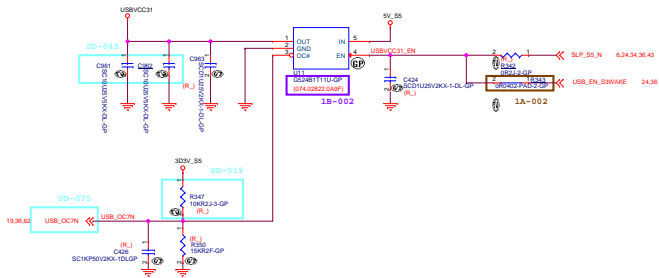


CTL1 SLP_S3#	CTL2 SLP_S4#	CTL3 GPIO41	ILIM_SEL GPIO41	Mode	State
0	0	0	0	Turn off power switch & discharge VBUS	S4/S5
0	0	1	1	DCP	S4/S5
0	1	0	0	SDP	S3
0	1	1	1	DCP with HID auto detect USB data pass through	S3
1	1	0	0	SDP	S0
1	1	1	1	CDP	S0

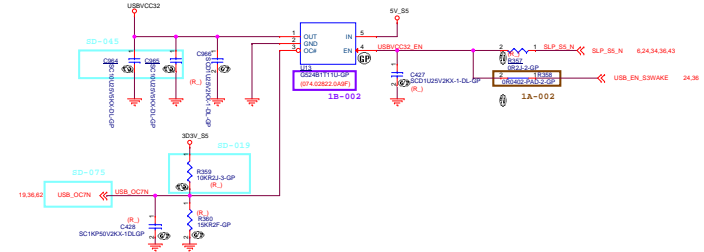


Rear I/O Charger

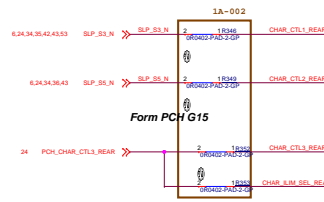
CPU USB 3.0*1+PCH USB2.0*1



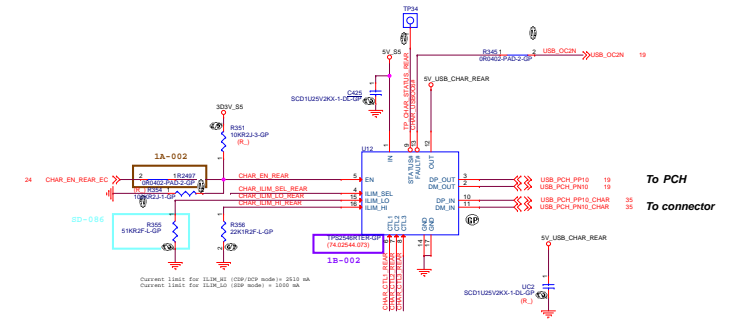
CPU USB 3.0*1+PCH USB2.0*1



Charger IC - TI TPS2546




CTL1 SLP_S#	CTL2 SLP_S#	CTL3 GPIO4	ILIM_SEL GPIO1	Mode	State
0	0	0	0	Turn off power switch & discharge VBUS	S4/S5
0	0	1	1	DCP	S4/S5
0	1	0	0	SDP	S3
0	1	1	1	DCP with HID auto detect USB data pass through	S3
1	1	0	0	SDP	S0
1	1	1	1	CDP	S0



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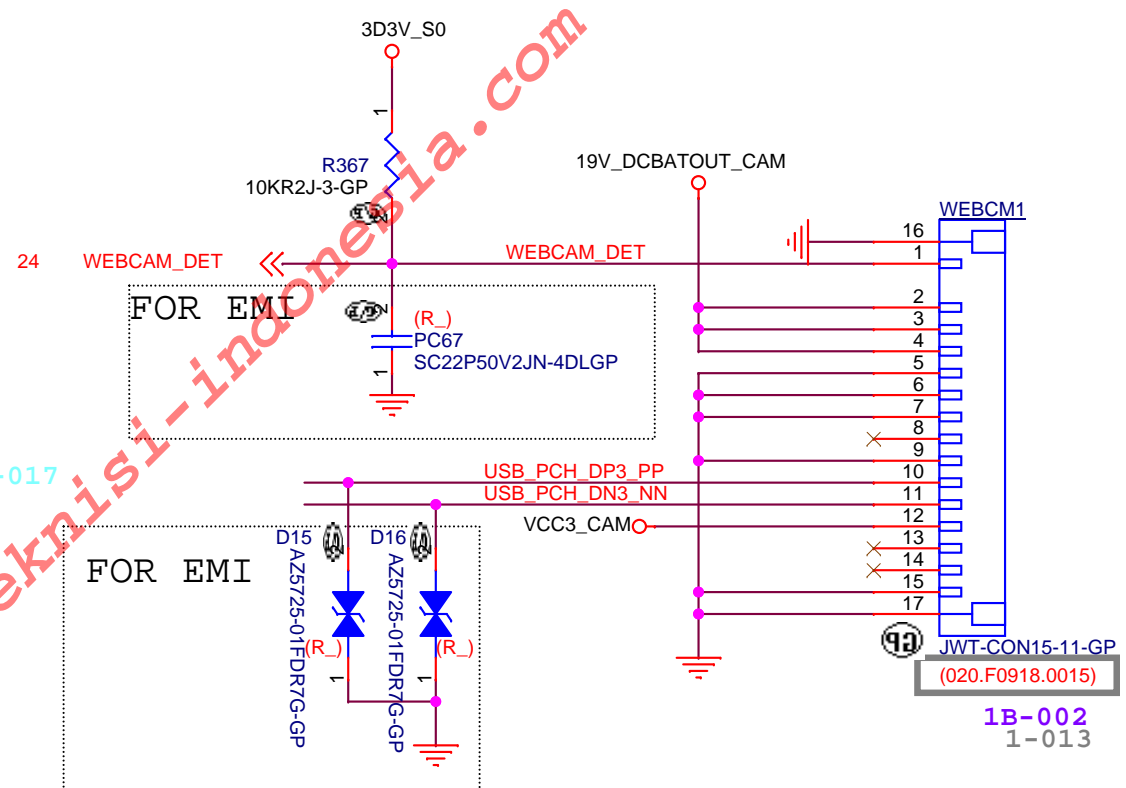
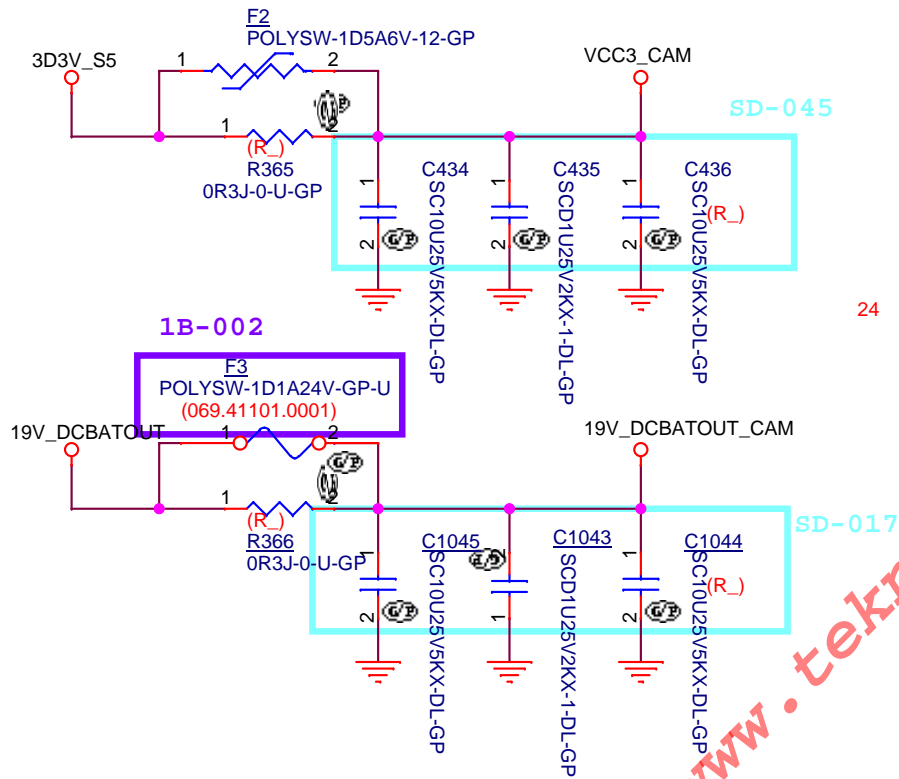
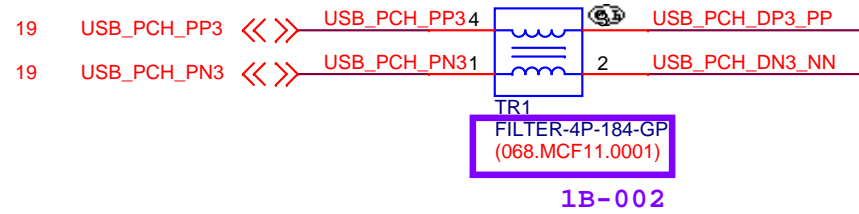
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WEBCAM



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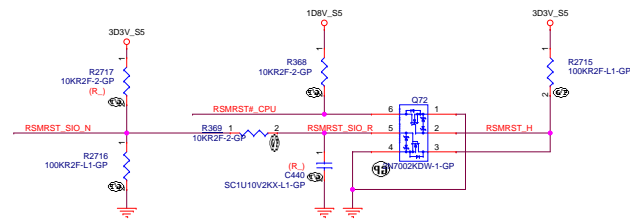
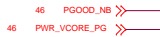
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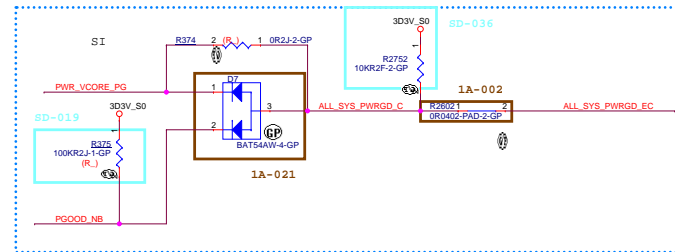
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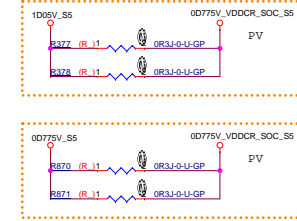
SVID



ALL_SYS_PWRGD



0D775V_VDDCR_SOC_S5



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S5_MUX_CTRL is an output signal from AM4 Type 0 processors that is used to multiplex (MUX) or control (CTRL) an external circuit to switch the VDDCR_SOC_S5 power rail between tracking VDDCR_SOC voltage during S0 and setting to a low power state during S3/S5.

~~VDDCR_SOC_S5 and S5_MUX_CTRL are not required for AM4 Type 2 or AM4 Type 3 processors.
Leave VDDCR_SOC_S5 and S5_MUX_CTRL unconnected for AM4 Type 2 or AM4 Type 3 processors.~~

For layout top and bottom the same

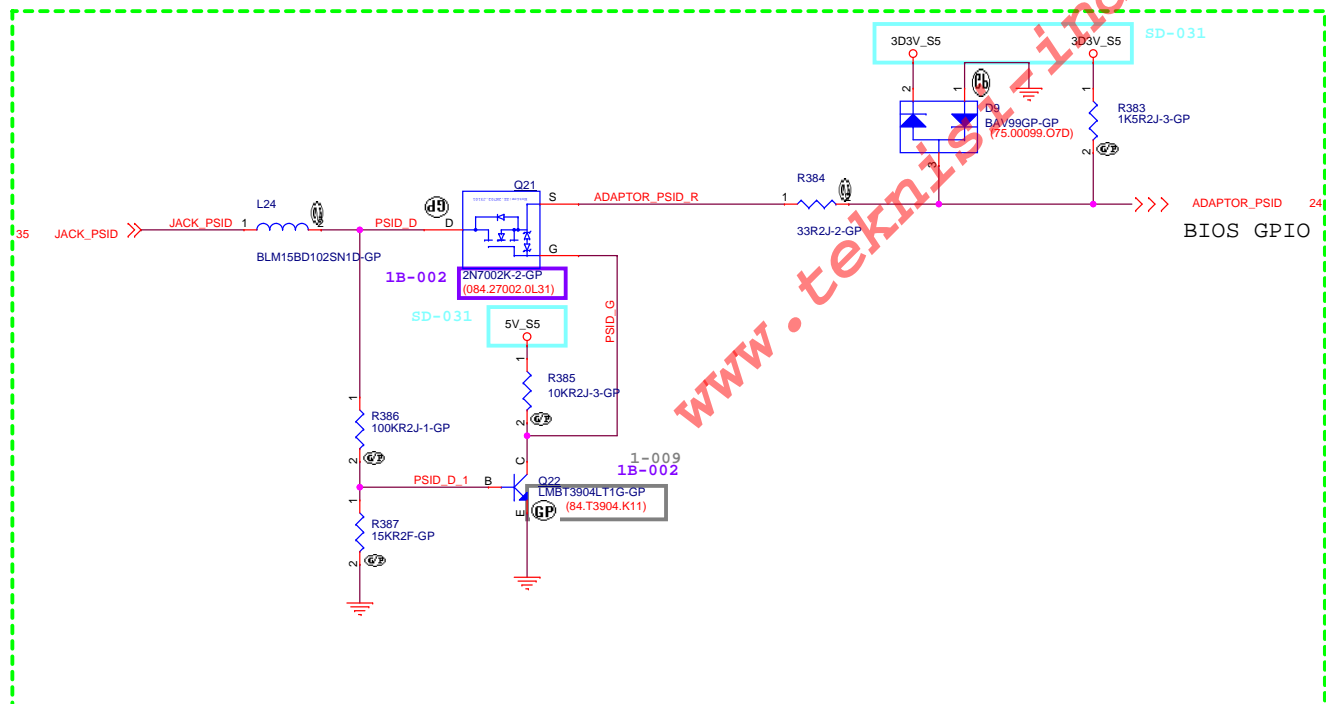
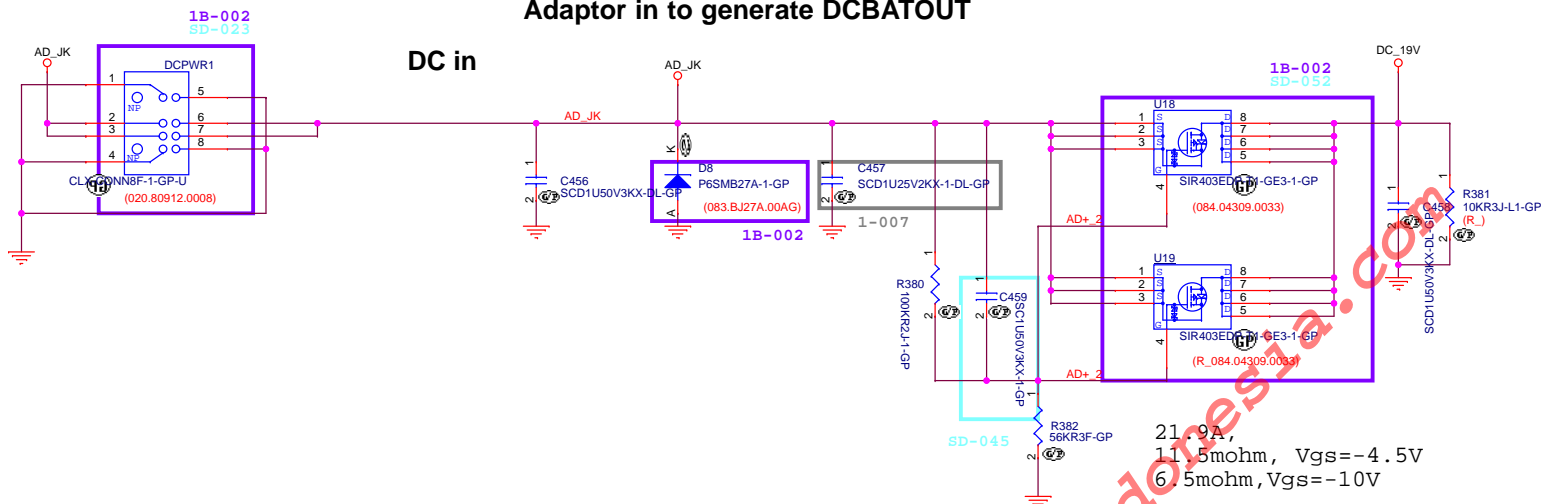
U33

R981 R982 R983

R1718

Adaptor in to generate DCBATOUT

DC in



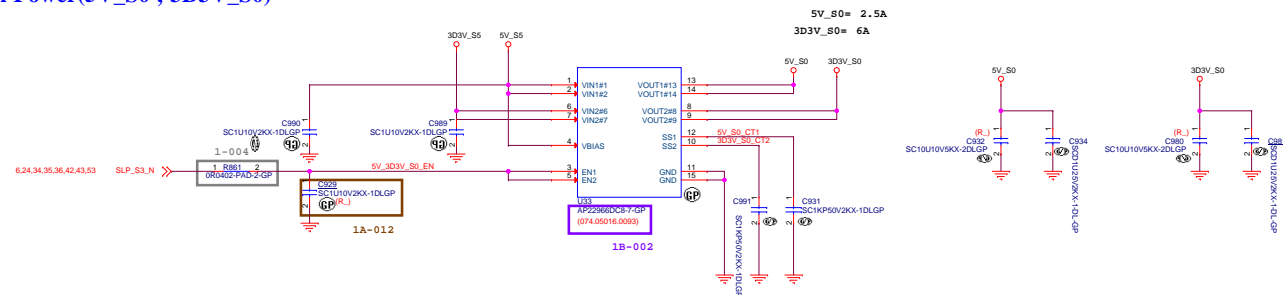
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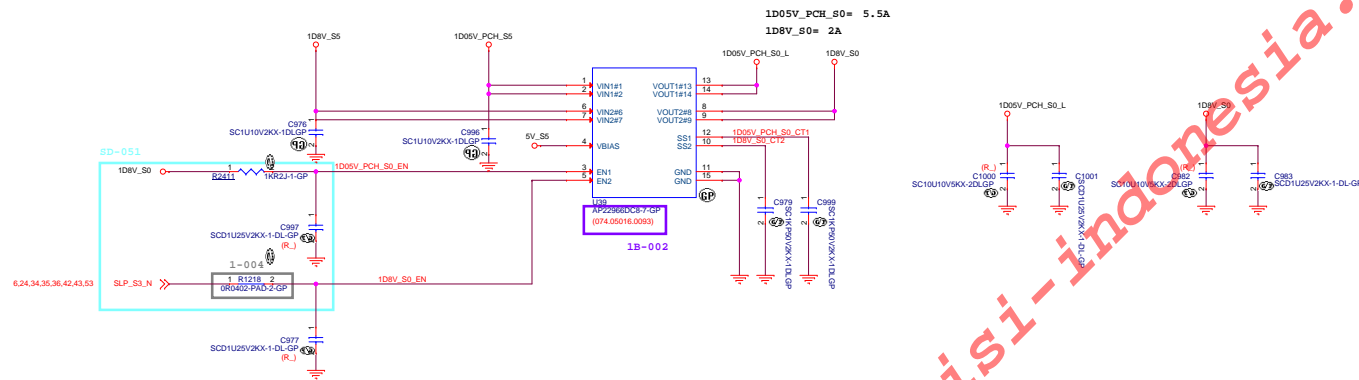
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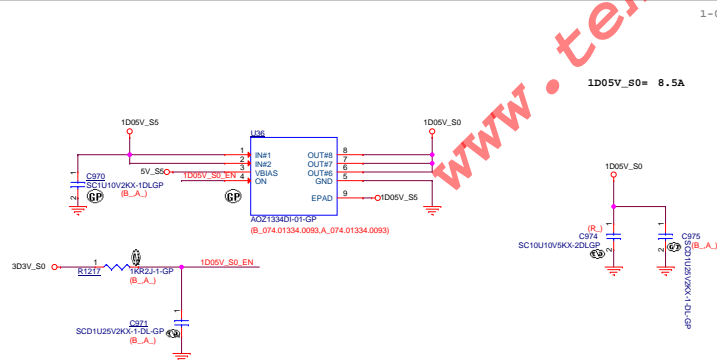
Run Power(1D05V_PCH_S0_L , 1D8V_S0)



Run Power(1D05V_PCH_S0_L , 1D8V_S0)

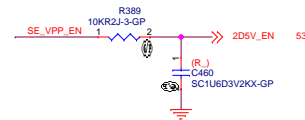
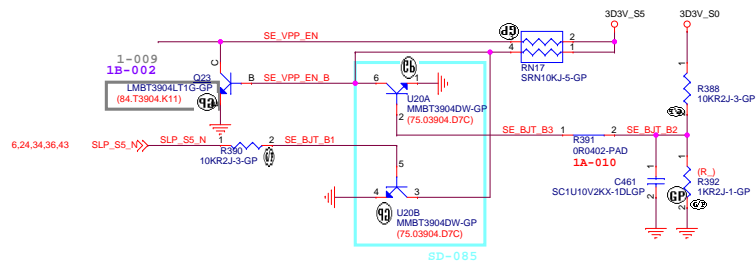


(Bristol only)

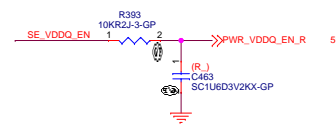
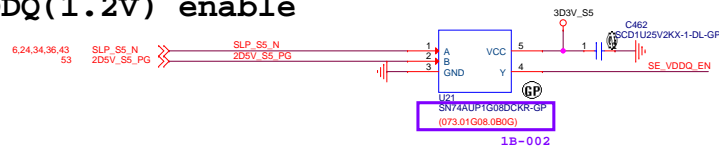


DDR4 Power Sequence

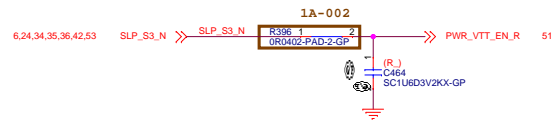
VPP(2.5V) enable



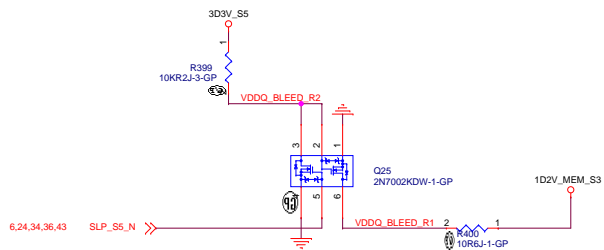
VDDQ(1.2V) enable



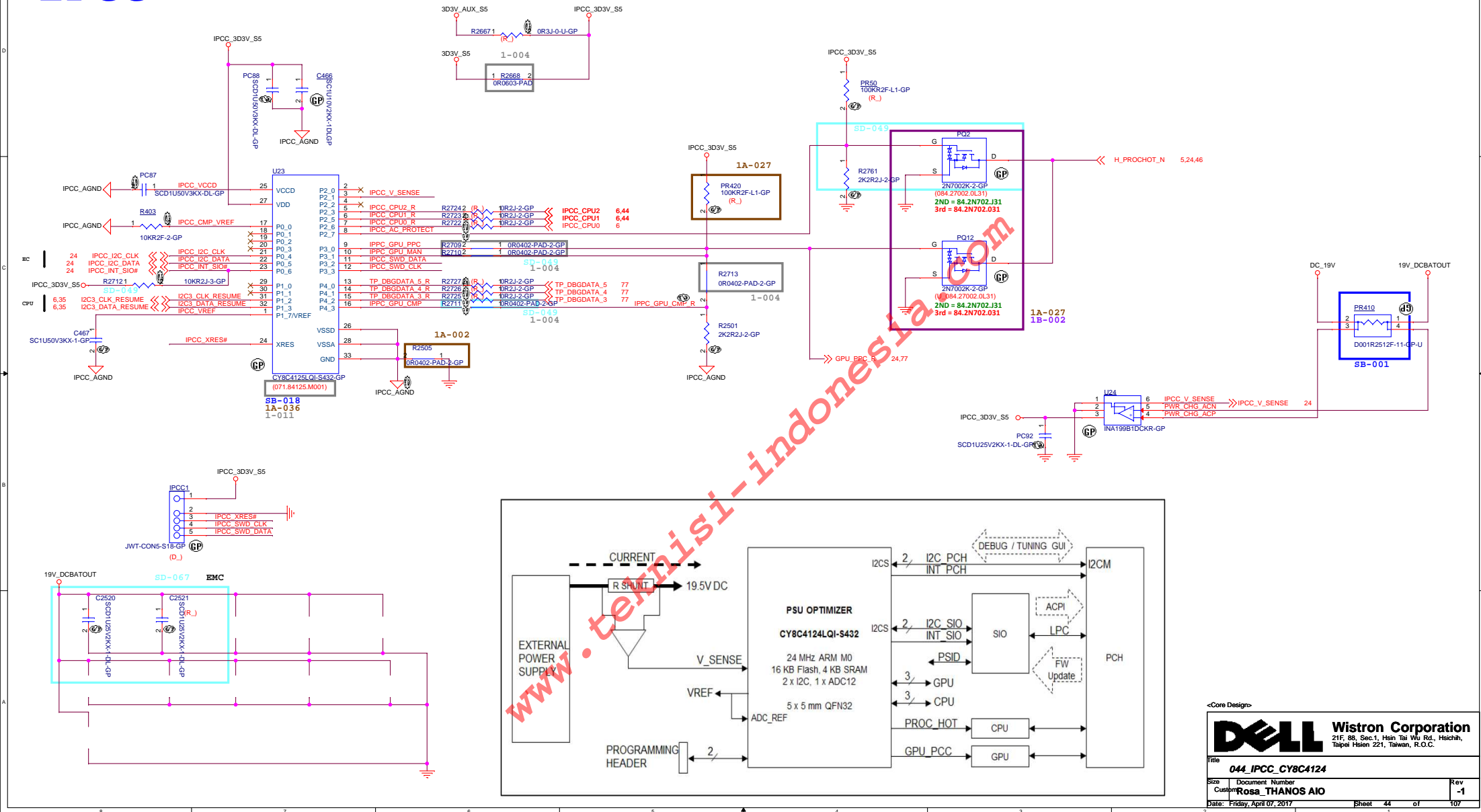
VTT(0.6V) enable



VDDQ discharge

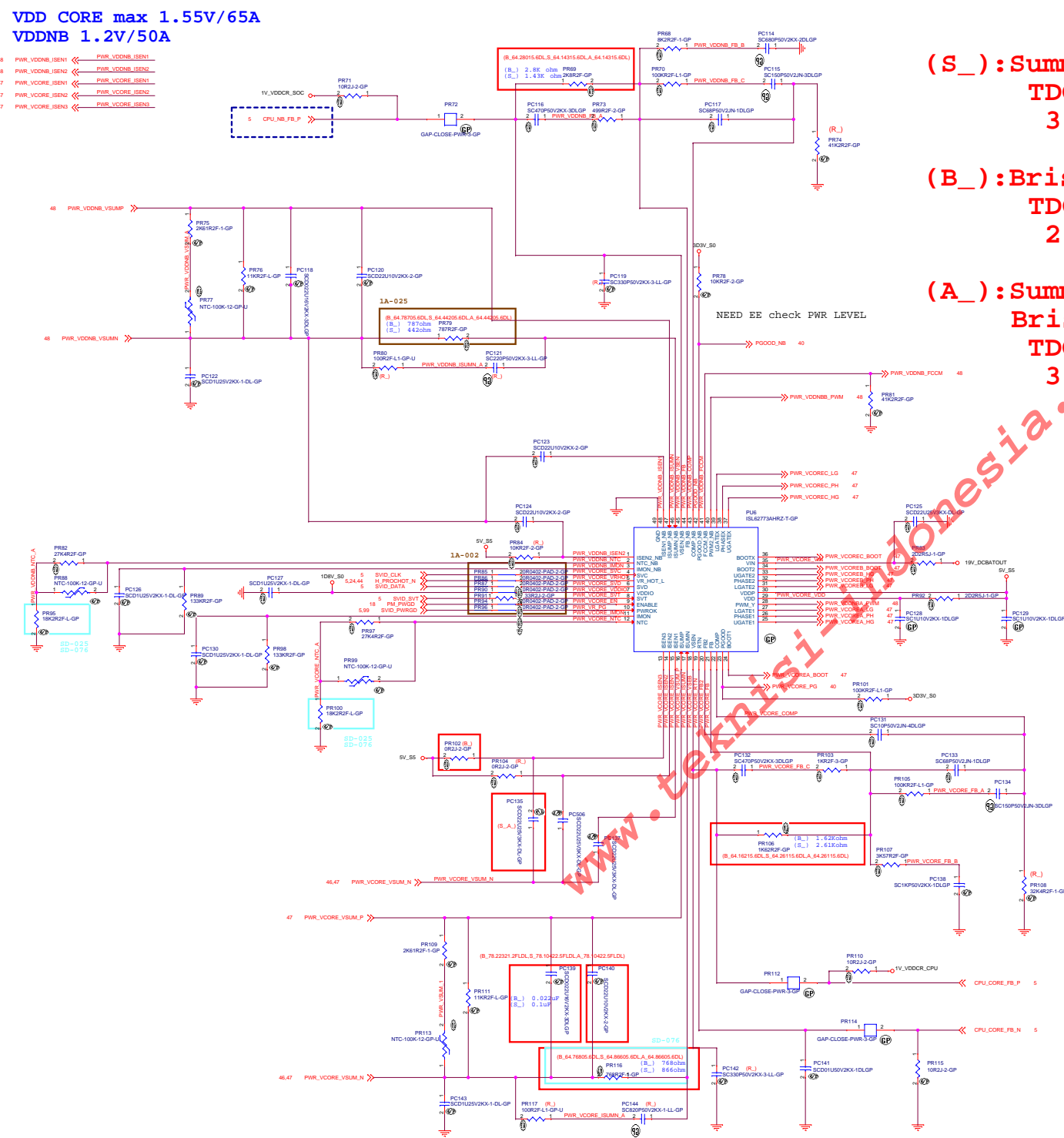


IPCC



VDD CORE max 1.55V/65A
VDDNB 1.2V/50A

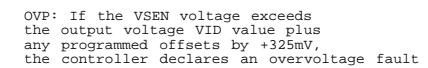
48 PWR_VDDNB_ISEN1 PWR_VDDNB_ISEN1
48 PWR_VDDNB_ISEN2 PWR_VDDNB_ISEN2
47 PWR_VCORE_ISEN1 PWR_VCORE_ISEN1
47 PWR_VCORE_ISEN2 PWR_VCORE_ISEN2
47 PWR_VCORE_ISEN3 PWR_VCORE_ISEN3



(S_):Summit Ridge (65W)
TDC:60A EDC:90A
3 phase

(B_):Bristol Ridge(35W)
TDC:39A EDC:55A
2 phase

(A_):Summit Ridge (65W)
Bristol Ridge(35W)
TDC:60A EDC:90A
3 phase

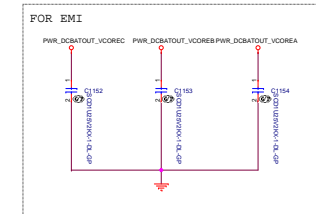


VDDRCR_CPU ,TDC=65AIMAX=90A,OCP>135A
PWM Frequency=300kHz
LIR=8.8A/30A=29%
330uF/2V, Ripple Current=3Arms
560uF/2.5V, Ripple Current=3.5Arms
Cout capacitance=3790uF

(S_):Summit Rigde (65W)
TDC:60A EDC:90A OCP>112.5A

(B_):Bristol Ridge(35W)
TDC:39A EDC:55A OCP>68.75A

(A_):Summit Ridge (65W)
Bristol Ridge(35W)

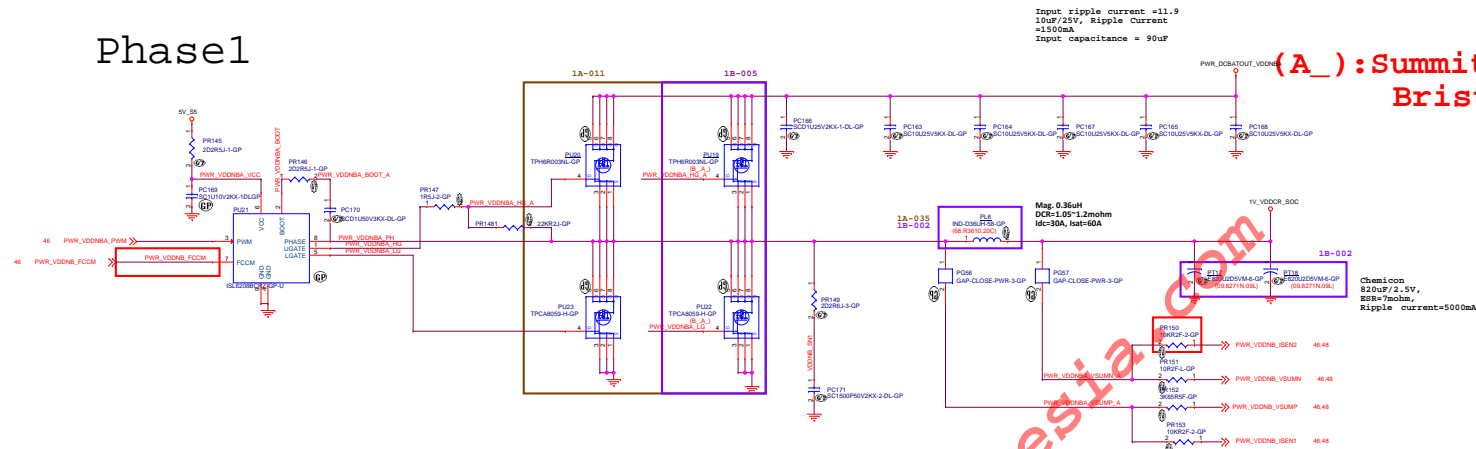


(S_):Summit Rigde (65W)
TDC:30A EDC:35A OCP>43.75A

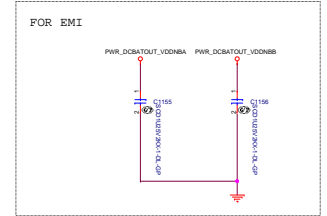
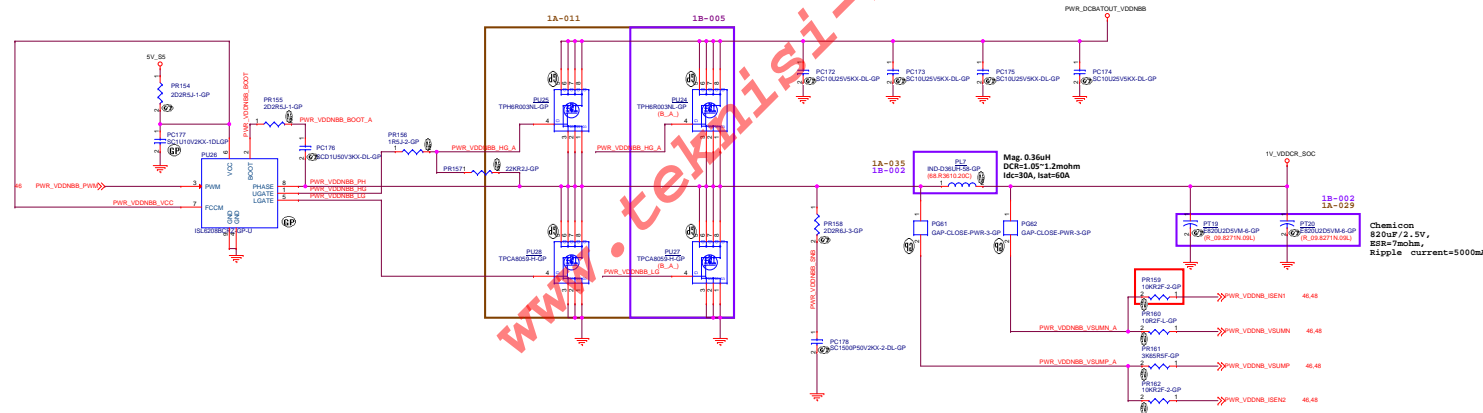
(B_):Bristol Ridge(35W)
TDC:40A EDC:60A OCP>75A

(A_):Summit Ridge (65W)
Bristol Ridge(35W)

Phase1




Phase2



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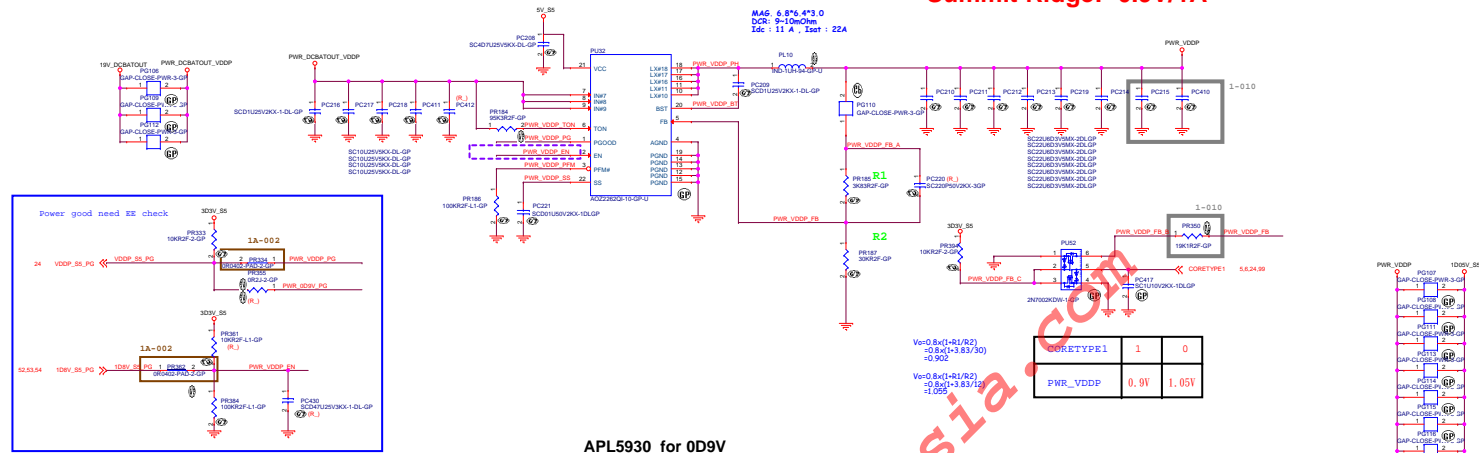
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PWR_VDDP_S5

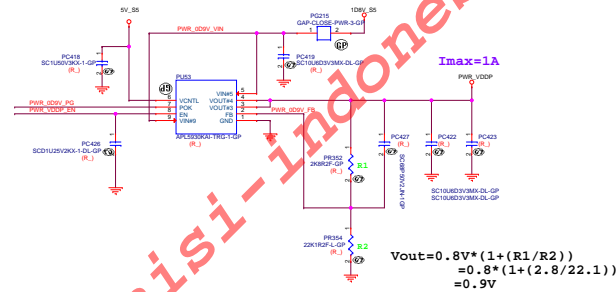
EE needs check sequence control

Bristol Ridge: 1.05V/9.5A
Summit Ridge: 0.9V/1A



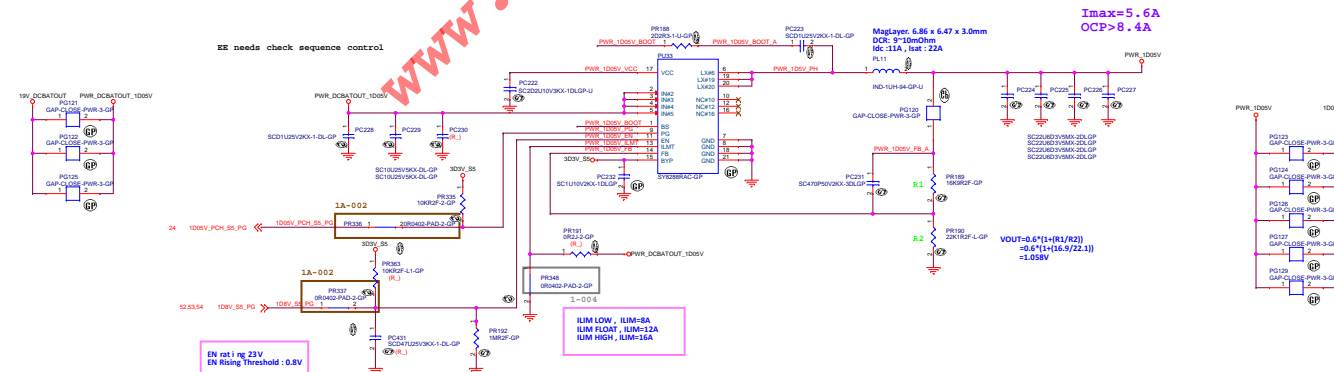
APL5930 for 0D9V

PWR_VDDP_S5 (0.9V)

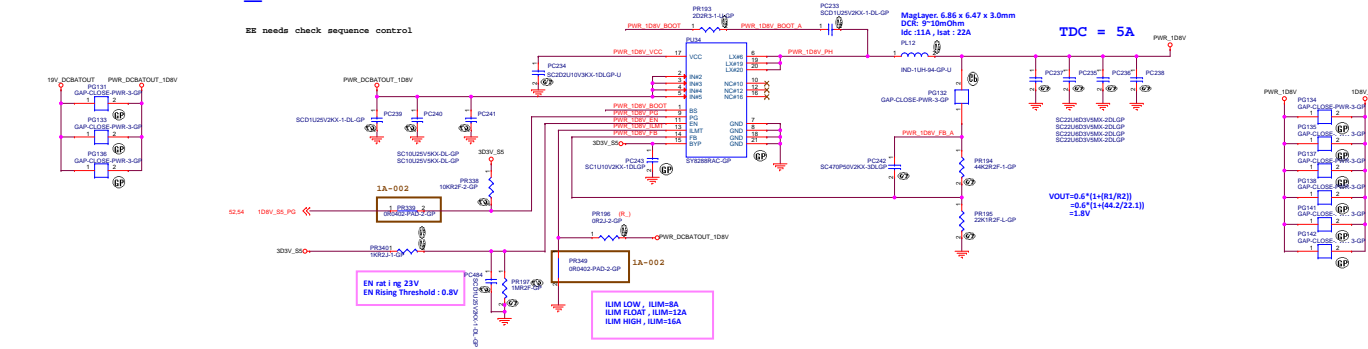


FCH 1D05V_S5

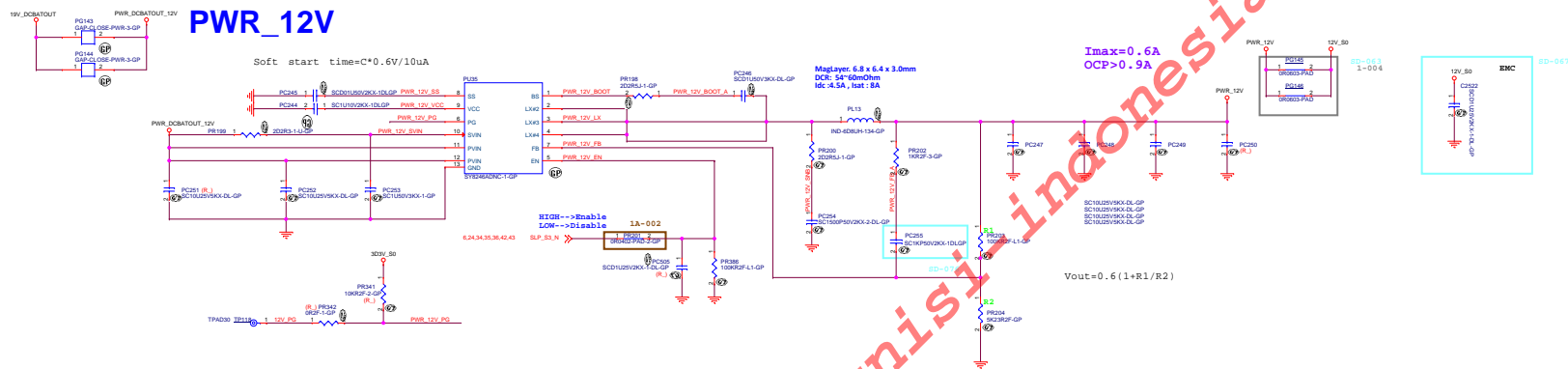
EE needs check sequence control



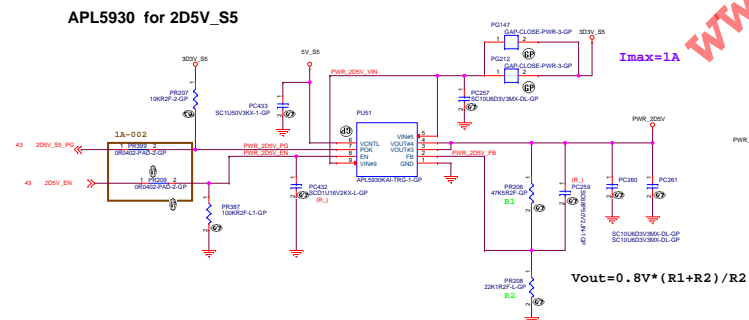
PWR_1D8V



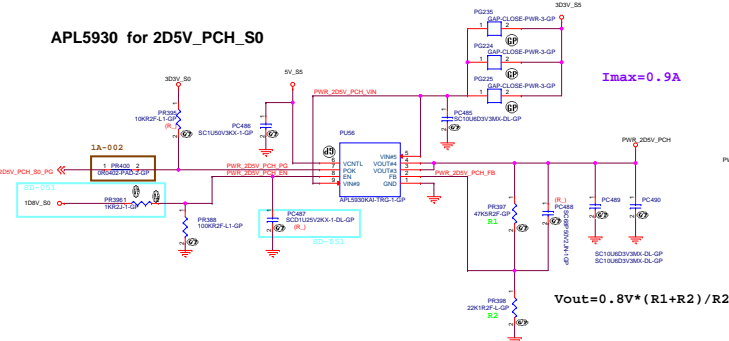
PWR_12V



PWR_2D5V_S5(2D5V_MEMVPP_S5)



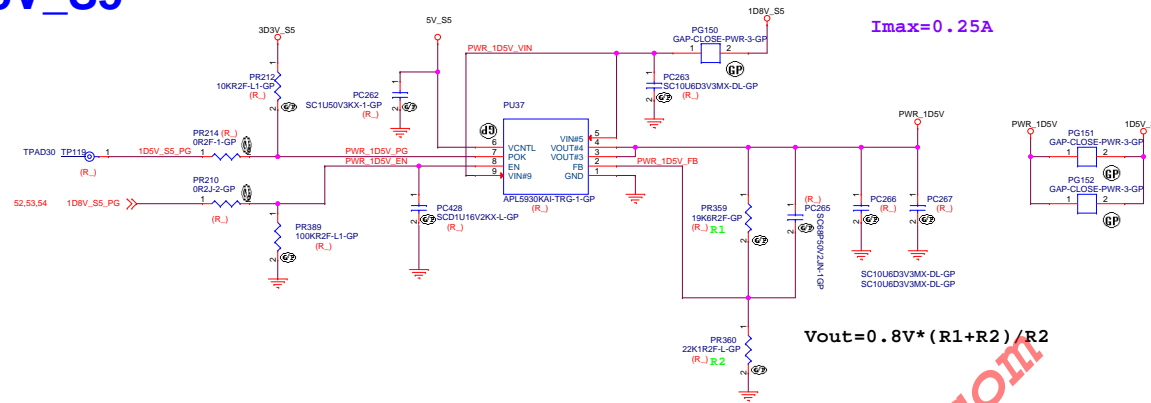
PWR_2D5V_PCH_S0



PWR_1D5V_S5

APL5930 for 1D5V

1A-008



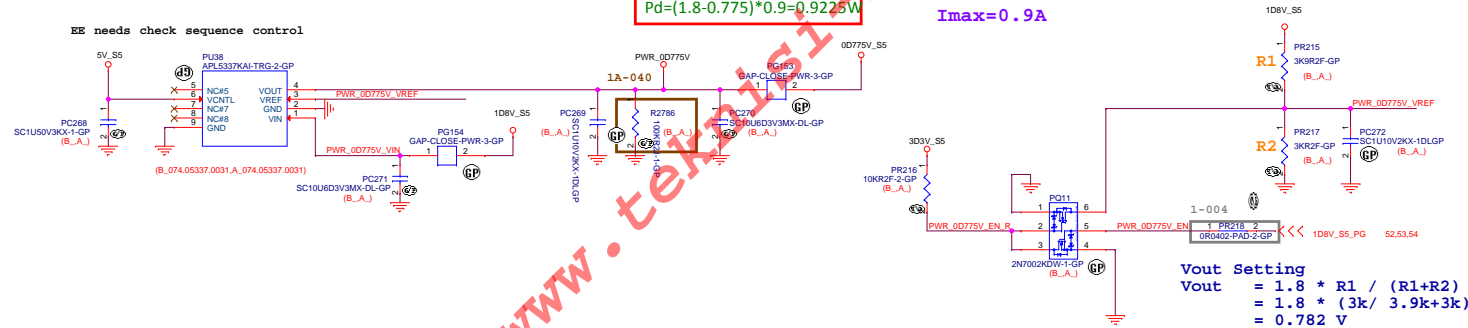
Imax=0.25A

$$V_{out} = 0.8V * (R1 + R2) / R2$$

Bristol Ridge only

PWR_0D775V

EE needs check sequence control



$$P_d = (1.8 - 0.775) * 0.9 = 0.9225W$$


Imax=0.9A

$$V_{out} \text{ Setting} = 1.8 * R1 / (R1 + R2) = 1.8 * (3k / 3.9k + 3k) = 0.782 V$$

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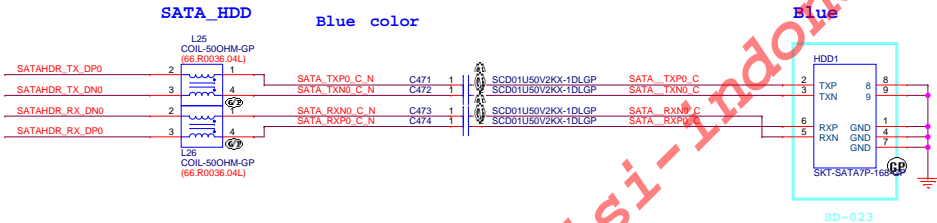
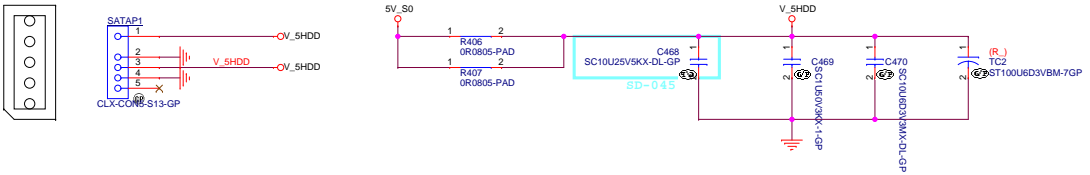
reference from KBL-U

SATA

- 17 SATAHDR_RX_DP0
- 17 SATAHDR_RX_DN0
- 17 SATAHDR_TX_DN0
- 17 SATAHDR_TX_DP0

SATA

Layout: Please put them together



PCIE WLAN

17 PCIE_RX_PCH_P0
17 PCIE_RX_PCH_N0
17 PCIE_TX_CON_P0
17 PCIE_TX_CON_N0

USB

19 USB_PCH_PP4
19 USB_PCH_PN4

PROM-WLAN

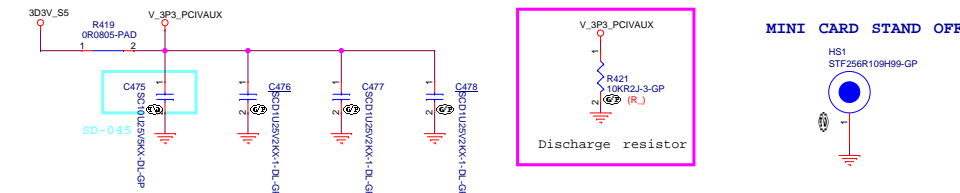
19 PEG_CLK0_WLAN_P
19 PEG_CLK0_WLAN_N
19 PEG_CLKREQ0_WLAN_C

EC

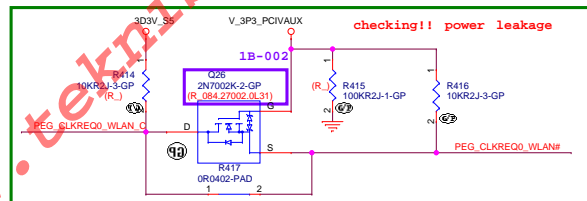
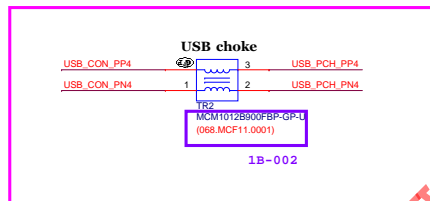
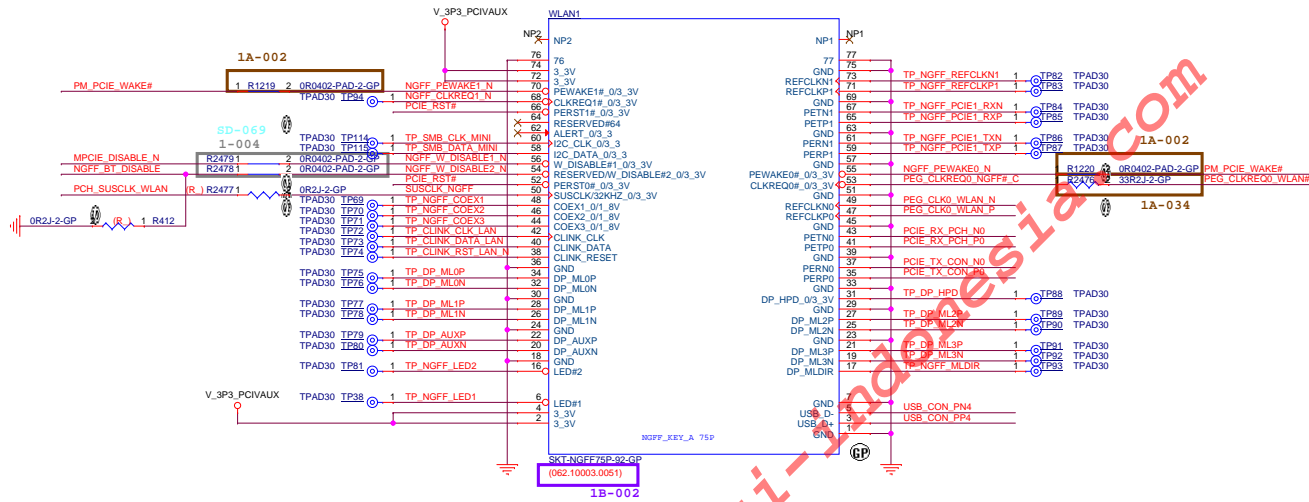
24 MPCIE_DISABLE_N
24 NGFF_BT_DISABLE

OTHERS

18,35,63 PM_PCIE_WAKE#
24 PCIE_RST#
18,24 PCH_SUSCLK_WLAN



NGFF(A Key)



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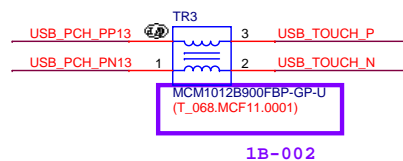
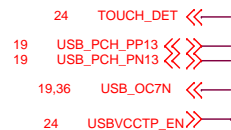
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061_M.2 (WLAN)_Key A

Size C Document Number
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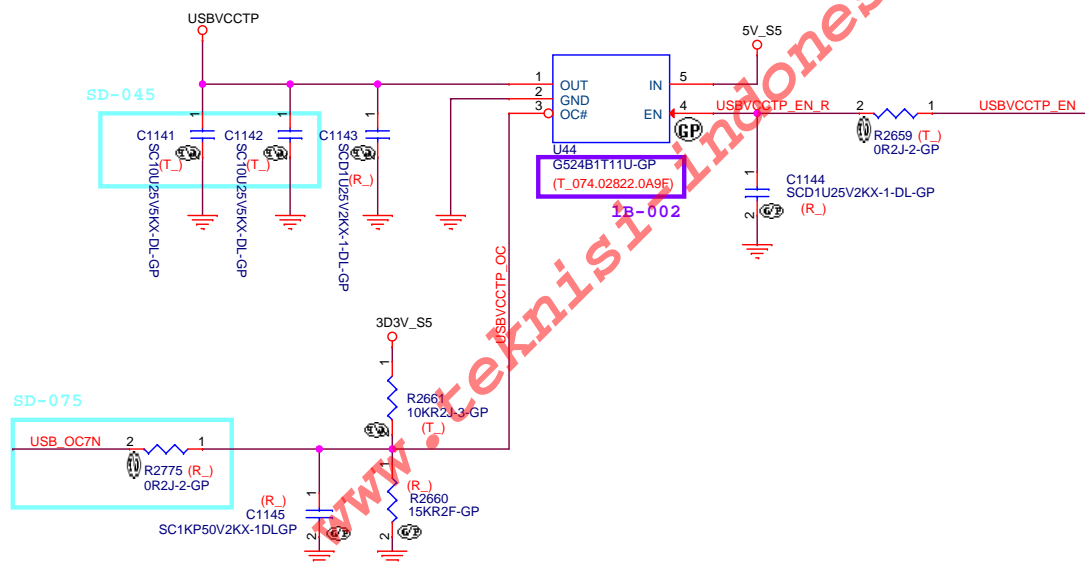
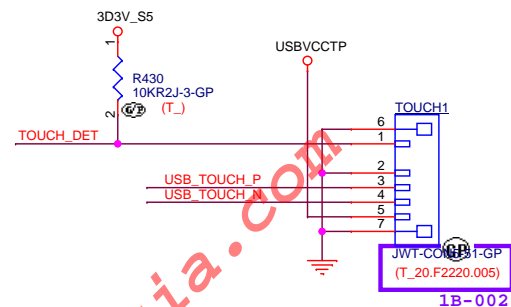
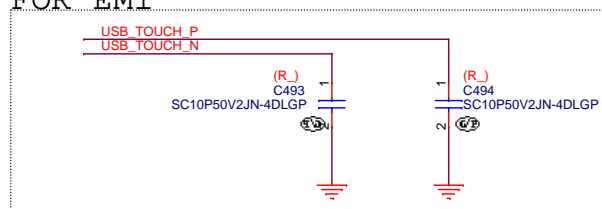
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TOUCH PANEL



FOR EMI



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062_TOUCH

Size
B

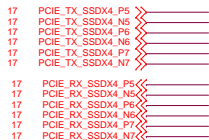
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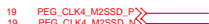
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PCIE SSD



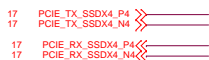
CLOCK



OTHER



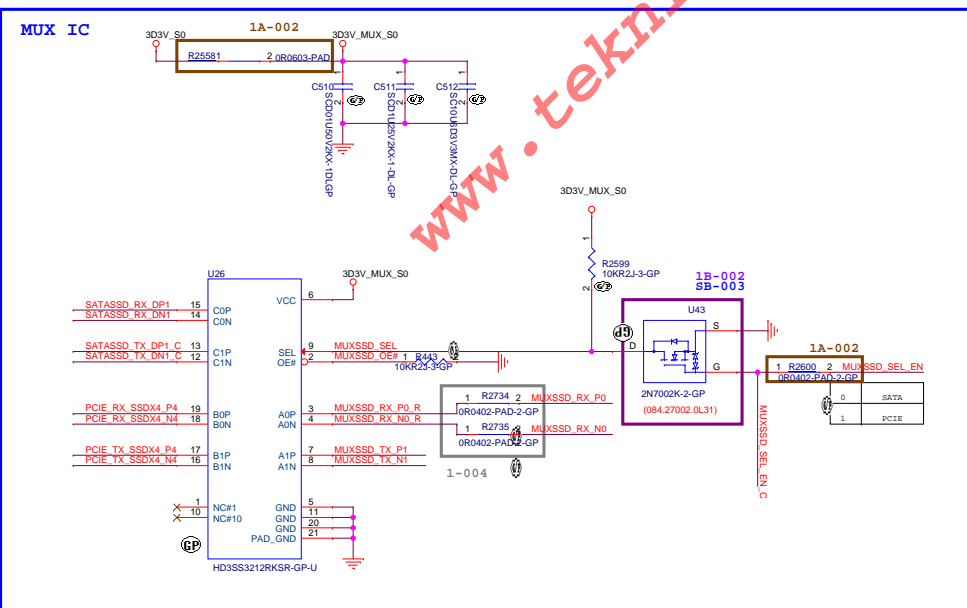
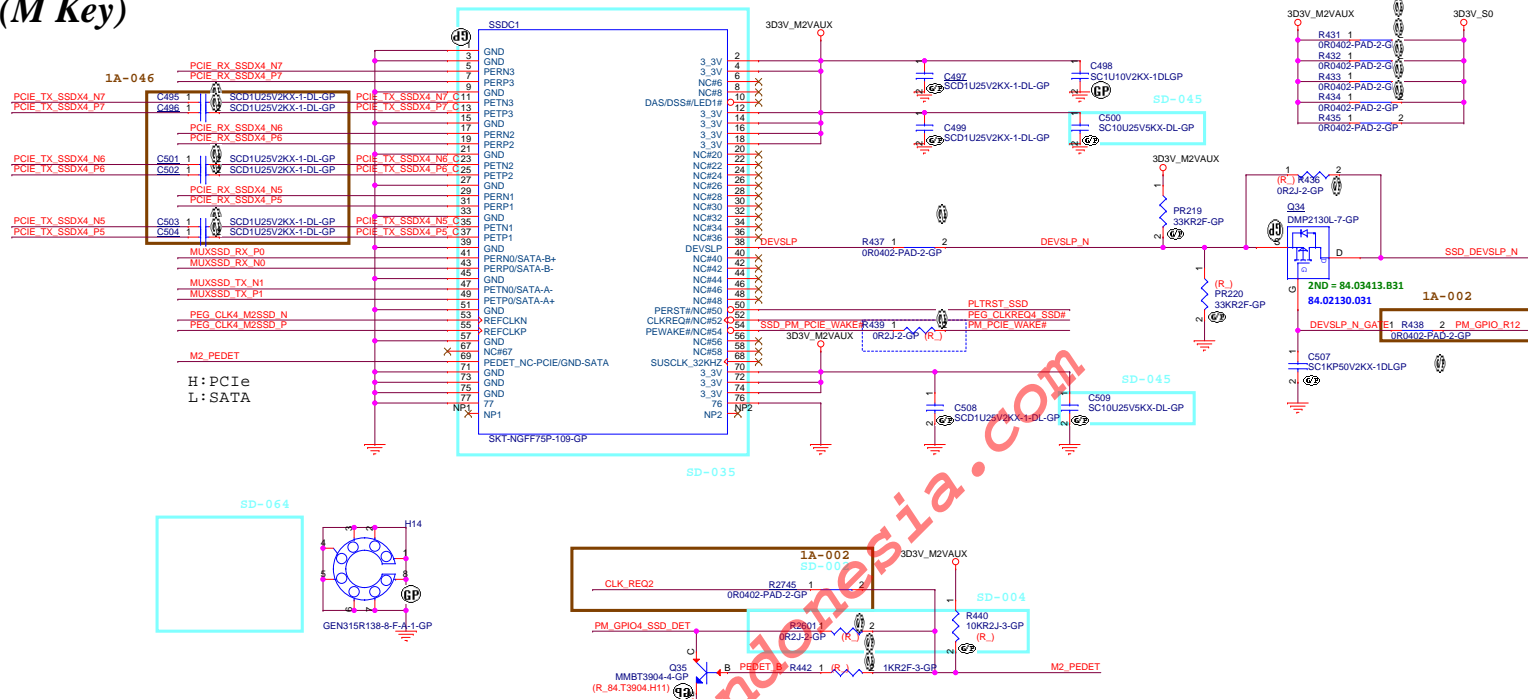
PCIE MUX SSD



SATA MUX SSD



SSD(M Key)



4.4. The SSD Slot; Slot C (Mechanical Key M)

This slot pin-out and key are only intended for SSD devices. The Host I/Fs supported are PCIe with up to 4 lanes or SATA. The state of the PEDET pin (67) will indicate to the platform which I/F of these two is actually connected.

74	3.3Vaux	GND	75
72	3.3Vaux	GND	73
70	3.3Vaux	GND	71
68	SUSCLK(32Hz) (O)(0/3.3V)	PEDET (OC-PCIe/GND-SATA)	69
	Key	N/C	67
	Key	Key	
	Key	Key	
	Key	Key	
58	N/C	GND	57
56	N/C	REFCLKP	55
54	PEWake# (IO)(0/3.3V) or N/C	REFCLKN	53
52	CLKREQ# (IO)(0/3.3V) or N/C	GND	51
50	PERST# (O)(0/3.3V) or N/C	PETp0/SATA-A+	49
48	N/C	PETn0/SATA-A-	47
46	N/C	GND	45
44	N/C	PERp0/SATA-B-	43
42	N/C	PERn0/SATA-B+	41
40	N/C	GND	39
38	DEVSLP (O)(0/3.3V)		

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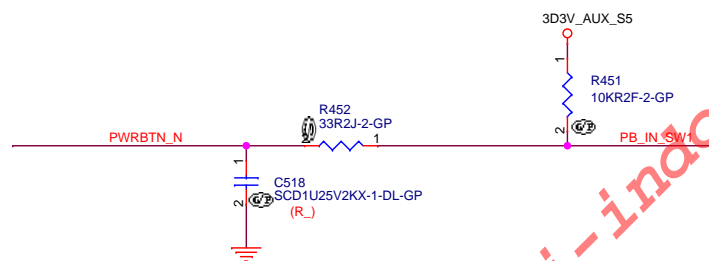
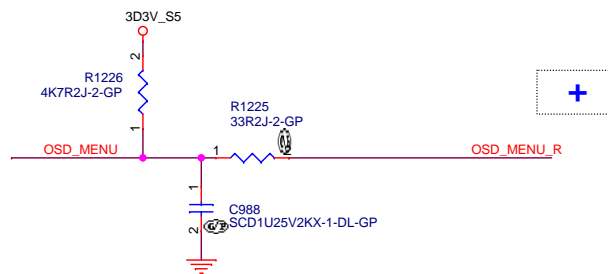
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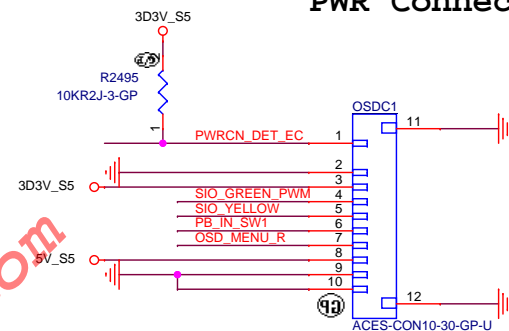
Power Botton/LED

- 24 PWRCN_DET_EC <<---
- 24 SIO_GREEN_PWM <<---
- 24 SIO_YELLOW >>---
- 7,24,35 OSD_MENU <<---
- 24 PWRBTN_N <<---

OSD Buttons



PWR Connector



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064_LED BOARD/POWER BUTTON			
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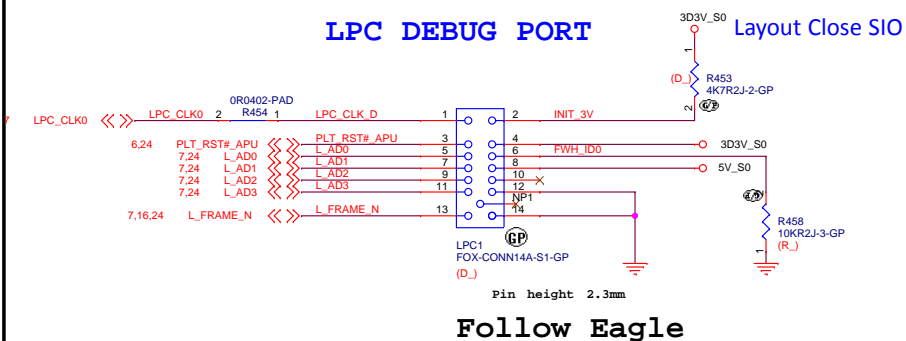
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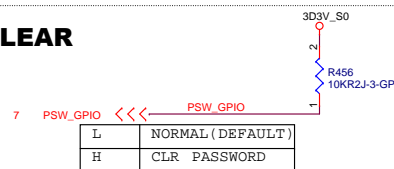
067_ (Reserved)

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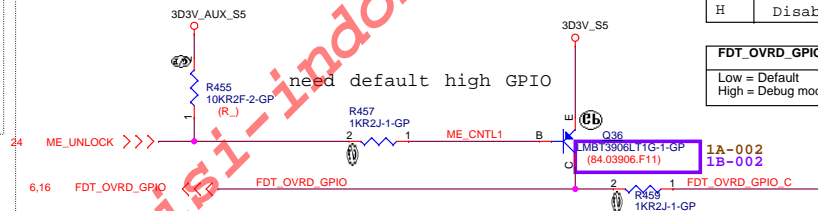
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PASSWORD CLEAR



ME ENABLE/DISABLE

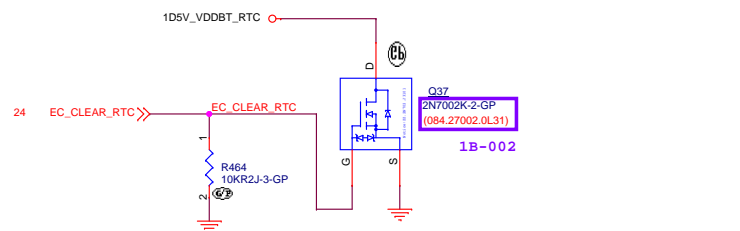
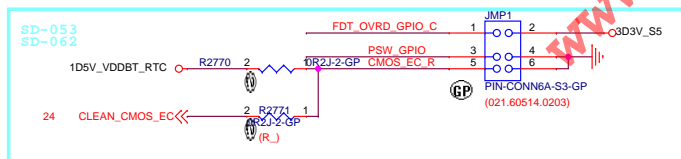


L	NORMAL (DEFAULT)
H	Disable

FDT_OVRD_GPIO
Low = Default High = Debug mode

CLEAN CMOS

With Jumper	Clear CMOS
Without Jumper	Normal Mode



Jumper	Function	Operation
JMP1	SERVICE_MODE	1 - 2 SHORT : Disable 1 - 2 OPEN : Default
	PASSWORD	3 - 4 SHORT : Default 3 - 4 OPEN : Clear
	CMOS	5 - 6 SHORT : Clear 5 - 6 OPEN : Default

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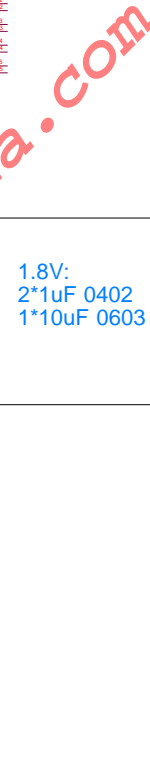
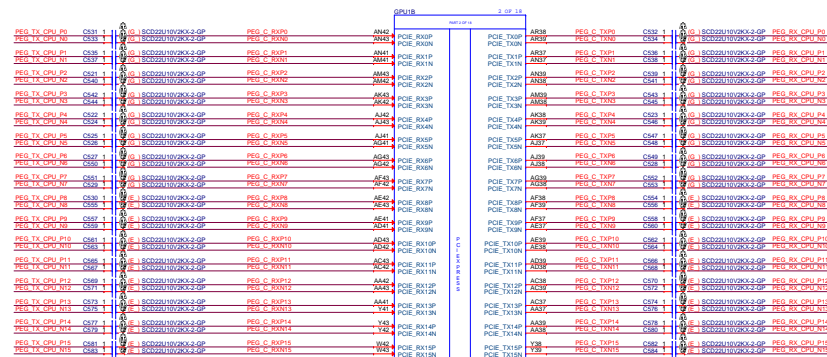
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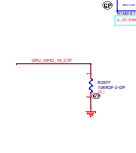
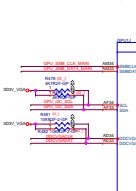
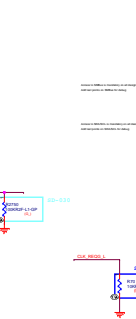
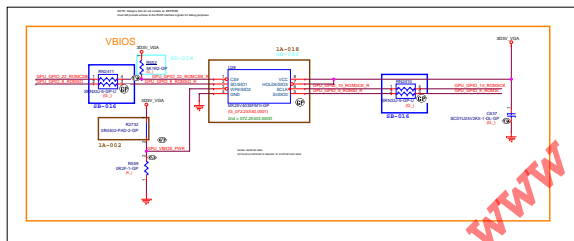
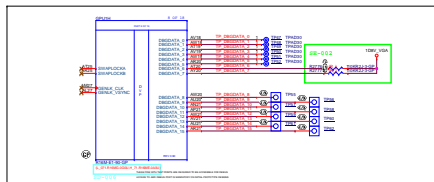
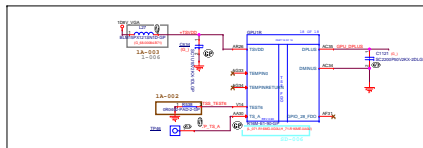
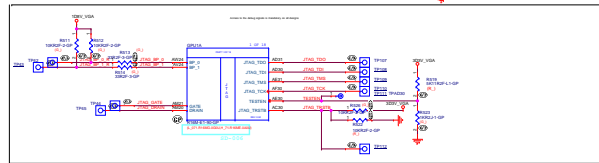
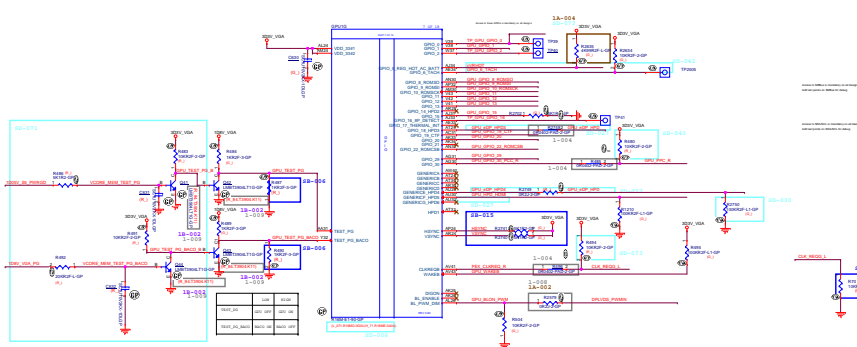
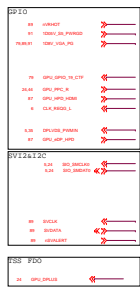
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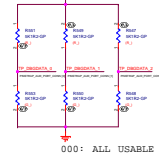
0.8V:
6*1uF 0402
1*0.1uF 0402
2*10uF 0603



GPU	115E/Version	TP_DATA_0	TP_DATA_1	TP_DATA_2	TP_DATA_3
01-00 (S0)	8074 B1000	0	0	1	0
01-00 (S0)	8074 B1000	1	0	1	0
01-00 (S0)	8074 B1000	0	0	0	0
01-00 (S0)	8074 B1000	1	0	1	0
01-00 (S0)	8074 B1000	1	1	1	0

Table 3-37 Primary Memory Aperture Size Requested at PCI Configuration	
Size of the Primary Memory Aperture	ROM_CONFIG(2:0)
128 MB	000
256 MB	001
512 MB	010
1 GB	011
2 GB	100
4 GB	101
8 GB	110
16 GB	111

PIN STRAPS



BIF_CLK_PM_EN	GPIO_8/ROMEN	Determine whether or not the PCIe reference clock power management capability is reported in the PCI configuration space (otherwise known as CLKREQB).	0 (Internal pull-down)	1 (Internal pull-up)
0: The CLKREQB power management capability is disabled.	0: The CLKREQB power management capability is disabled.	1: The CLKREQB power management capability is enabled.	0: Design dependent, see description.	1: Provide a pull-up resistor option to VDD_33 on the PCB for each pin.

BIF_GEN3_ENA	GPIO_2	PCIe Gen3 capability.	1 (Internal pull-up)	0 (Internal pull-down)
0: PCIe Gen3 is not supported.	0: PCIe Gen3 is not supported.	1: PCIe Gen3 is supported.	1: Provide a pull-up resistor option to VDD_33 on the PCB for each pin.	0: Design dependent, see description.

BIF_VGA_DIS	GPIO_29	Determine whether or not the card will be recognized as the system's VGA controller (via the SUBCLASS field in the PCI configuration space).	0 (Internal pull-down)	1 (Internal pull-up)
0: VGA Controller capacity enabled.	0: VGA Controller capacity enabled.	1: The device will not be recognized as the system's VGA controller (for headless designs).	0: Design dependent.	1: Provide a pull-up resistor option to VDD_33 on the PCB for each pin.

BIOS_ROM_EN	GPIO_22/ROMCSB	Enable external BIOS ROM device.	0 (Internal pull-up)	1 (Internal pull-down)
0: Disable external BIOS ROM device.	0: Disable external BIOS ROM device.	1: Enable external BIOS ROM device.	0: Design dependent.	1: Provide a pull-down resistor option to GND on the PCB for each pin.

BOARD_CONFIG	DBGDAT_5	Provides an option to specify certain board-level specifics to the VBIOS or driver.	0 (Internal pull-down)	1 (Internal pull-up)
0: Provide a pull-up resistor option to VDD_18 on the PCB for each pin.	0: Provide a pull-up resistor option to VDD_18 on the PCB for each pin.	1: Provide a pull-up resistor option to VDD_18 on the PCB for each pin.	0: Design dependent.	1: Provide a pull-down resistor option to GND on the PCB for each pin.

ROM_CONFIG(2:0)	GPIO_13	GPIO_12	GPIO_11	a) If BIOS_ROM_EN = 1, then ROM_CONFIG(2:0) defines the ROM type. See ROM Configurations (p. 42) for details.	0 (Internal pull-up)	1 (Internal pull-down)
0: Provide a pull-up resistor option to VDD_33 on the PCB for each pin.	0: Provide a pull-up resistor option to VDD_33 on the PCB for each pin.	0: Provide a pull-up resistor option to VDD_33 on the PCB for each pin.	0: Provide a pull-up resistor option to VDD_33 on the PCB for each pin.	1: Provide a pull-up resistor option to VDD_33 on the PCB for each pin.	0: Design dependent.	1: Provide a pull-down resistor option to GND on the PCB for each pin.

SMBUS_ADDR	GPIO_1	Provides a strap option to change the SMBUS slave address of the GPU.	0 (Internal pull-down)	1 (Internal pull-up)
0: 0x40	0: 0x40	1: 0x41	0: Design dependent.	1: Provide a pull-up resistor option to VDD_33 on the PCB for each pin.

TX_DEEMPH_EN	GPIO_20	PCI Express transmitter de-emphasis enable.	0 (Internal pull-down)	1 (Internal pull-up)
0: Tx de-emphasis disabled.	0: Tx de-emphasis disabled.	1: Tx de-emphasis enabled.	0: Design dependent.	1: Through pull-up resistor to VDD_33.

TX_HALF_SWING	GPIO_0	Controls the transmitter full-half swing mode.	0 (Internal pull-down)	1 (Internal pull-up)
0: The transmitter full-swing is enabled.	0: The transmitter full-swing is enabled.	1: The transmitter half-swing is enabled.	0: Design dependent.	1: Provide a pull-up resistor option to VDD_33 on the PCB for each pin.

Reserved	GPIO_9/ROMSI	Reserved	0 (Internal pull-down)	1 (Internal pull-up)
0: Must default to 0 for production.	0: Must default to 0 for production.	1: Provide a pull-up resistor option to VDD_33 on the PCB for each pin.	0: Design dependent.	1: Provide a pull-up resistor option to VDD_33 on the PCB for each pin.

a All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/us.
 b The VDD_18 rail must reach its ready status at least 10 us before VDDC and VDDV_18 start to ramp-up.
 c For power down, reversing the ramp-up sequence is recommended.

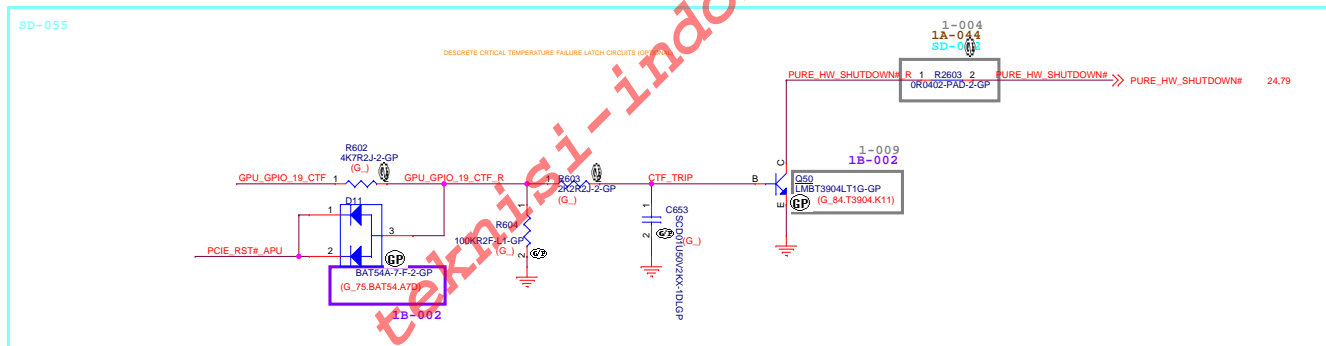
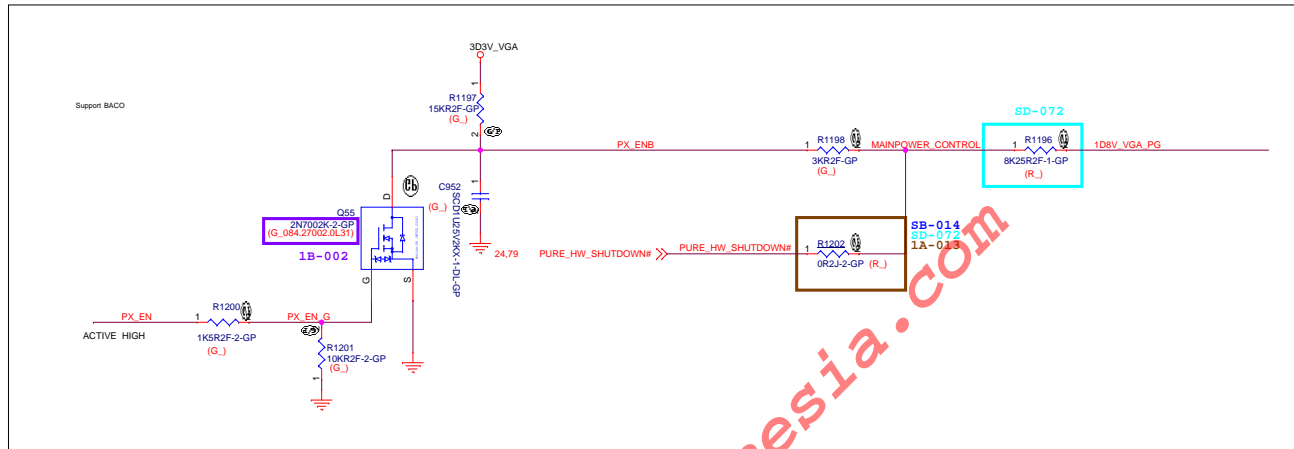
COMPONENTS SHOWN ARE EXAMPLES ONLY
AND NOT NECESSARILY QUALIFIED

BACO mode

76 PX_EN >>
 77,89,91 1D8V_VGA_PG <<
 24,79 PURE_HW_SHUTDOWN# <<

CTF

77 GPU_GPIO_19_CTF >>
 6,18,76,89 PCIE_RST#_APU >>
 24,79 PURE_HW_SHUTDOWN# <<



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Title 079_GPU_Thermal & BACO & CTF
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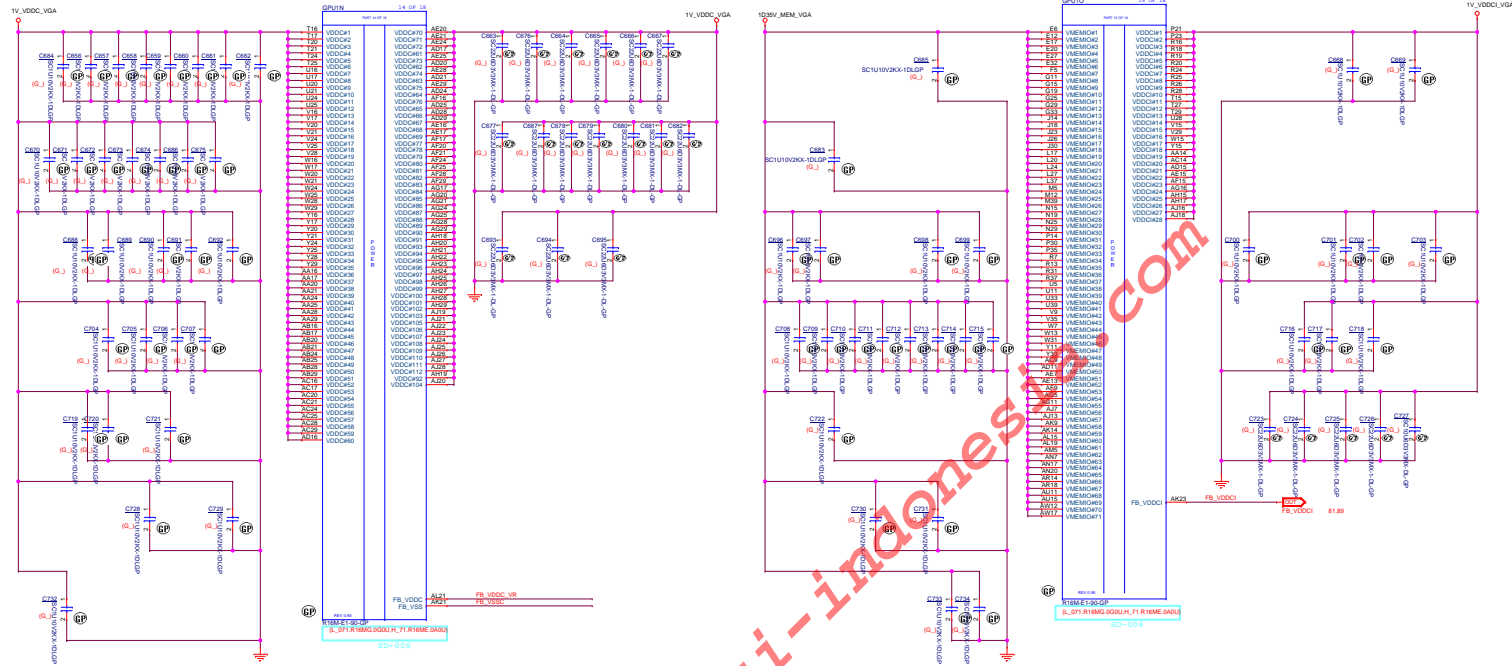
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Title: **080_GPU_GND**

Size: C Document Number: **Rosa_THANOS AIO** Rev: **-1**

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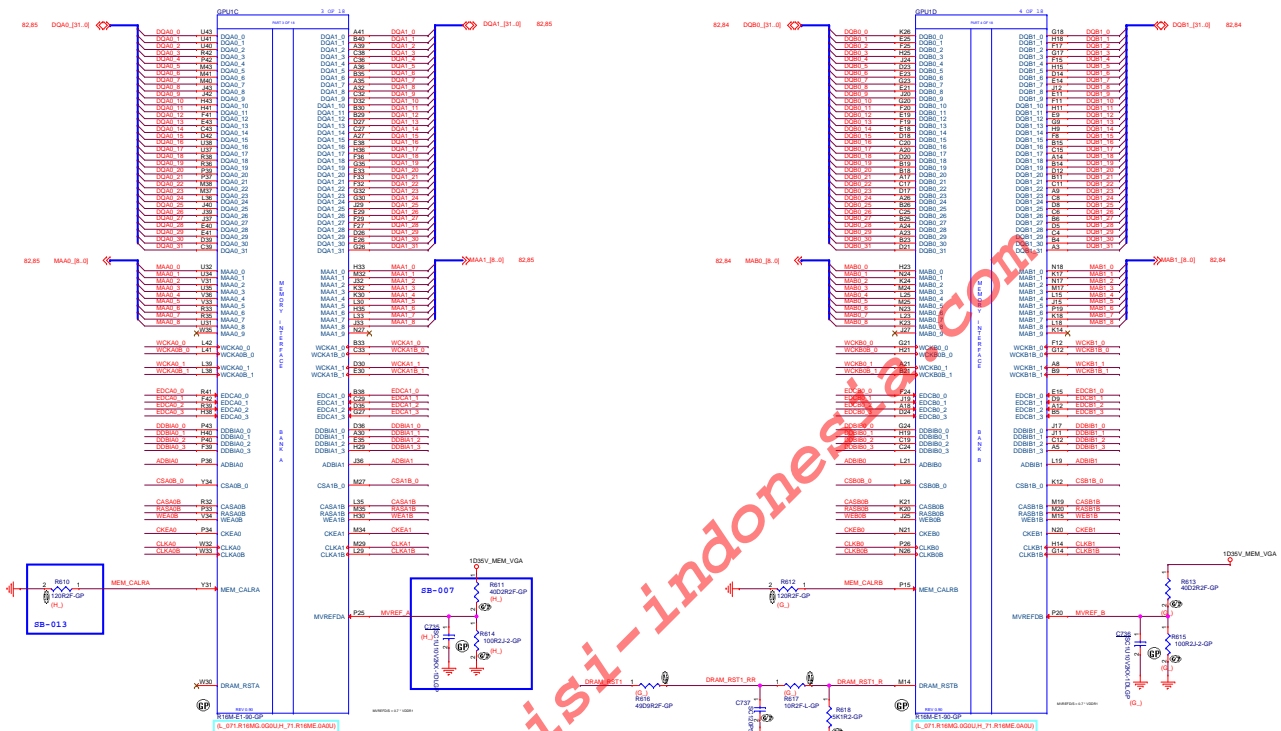
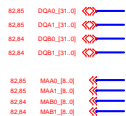
80 FB_VDDC_VR
80 FB_VSSC
81.80 FB_VDDCI



1V_VDDC_VGA:
30*1uF 0402
16*22uF 0603

1V_VDDCI_VGA:
9*1uF 0402
4* 22uF 0603
1* 10uF 0805

1D35V_MEM_VGA:
19*1uF 0402



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83.85 DQ00_[31:0] <>
 83.85 DQ01_[31:0] <>
 83.84 DQ02_[31:0] <>
 83.84 DQ03_[31:0] <>

 83.85 MAC0_[8:0] <>
 83.85 MAC1_[8:0] <>
 83.84 MAC0_[8:0] <>
 83.84 MAC1_[8:0] <>

C0

85 WORK0_0 <>
 85 WORK0B_0 <>
 85 WORK0B_1 <>
 85 EDC00_0 <>
 85 EDC00_1 <>
 85 EDC00_2 <>
 85 EDC00_3 <>
 85 DDB00_0 <>
 85 DDB00_1 <>
 85 DDB00_2 <>
 85 DDB00_3 <>
 85 ADB00 <>
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 85 CAS00B <>
 85 RAS00B <>
 85 WE00B <>
 85 CK000 <>
 85 CLK00 <>
 85 CLK00B <>

C1

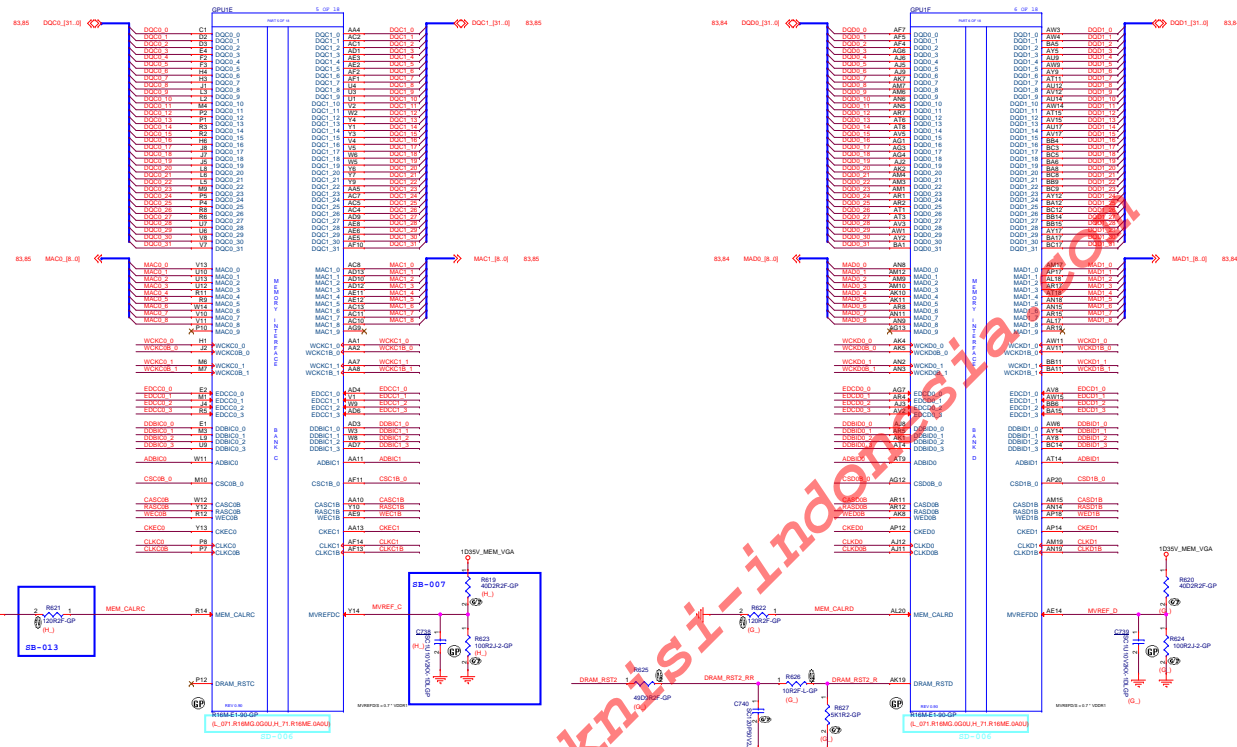
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 85 DDB01_1 <>
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 85 DDB01_3 <>
 85 ADB01 <>
 85 CS01B_0 <>
 85 CAS01B <>
 85 RAS01B <>
 85 WE01B <>
 85 CK001 <>
 85 CLK01 <>
 85 CLK01B <>

D0

84 WORK0_0 <>
 84 WORK0B_0 <>
 84 WORK0B_1 <>
 84 EDC00_0 <>
 84 EDC00_1 <>
 84 EDC00_2 <>
 84 EDC00_3 <>
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 84 DDB00_1 <>
 84 DDB00_2 <>
 84 DDB00_3 <>
 84 ADB00 <>
 84 CS00B_0 <>
 84 CAS00B <>
 84 RAS00B <>
 84 WE00B <>
 84 CK000 <>
 84 CLK00 <>
 84 CLK00B <>
 84.85 DRAM_RST0 <>

D1

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 84 WORK0B_0 <>
 84 WORK0B_1 <>
 84 EDC01_0 <>
 84 EDC01_1 <>
 84 EDC01_2 <>
 84 EDC01_3 <>
 84 DDB01_0 <>
 84 DDB01_1 <>
 84 DDB01_2 <>
 84 DDB01_3 <>
 84 ADB01 <>
 84 CS01B_0 <>
 84 CAS01B <>
 84 RAS01B <>
 84 WE01B <>
 84 CK001 <>
 84 CLK01 <>
 84 CLK01B <>



24 RDISPLAY2_DET_EC <<>> RDISPLAY2_DET_EC

HDMI

86 GPU_HDMI_OUT0p << GPU_HDMI_OUT0p
86 GPU_HDMI_OUT0n << GPU_HDMI_OUT0n
86 GPU_HDMI_OUT1p << GPU_HDMI_OUT1p
86 GPU_HDMI_OUT1n << GPU_HDMI_OUT1n
86 GPU_HDMI_OUT2p << GPU_HDMI_OUT2p
86 GPU_HDMI_OUT2n << GPU_HDMI_OUT2n
86 GPU_HDMI_OUT_CKp << GPU_HDMI_OUT_CKp
86 GPU_HDMI_OUT_CKn << GPU_HDMI_OUT_CKn

86 GPU_HDMI_OUT_SCL << GPU_HDMI_OUT_SCL
86 GPU_HDMI_OUT_SDA <<>> GPU_HDMI_OUT_SDA

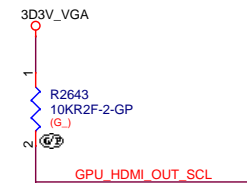
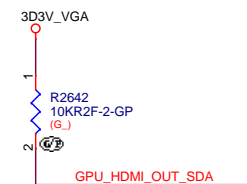
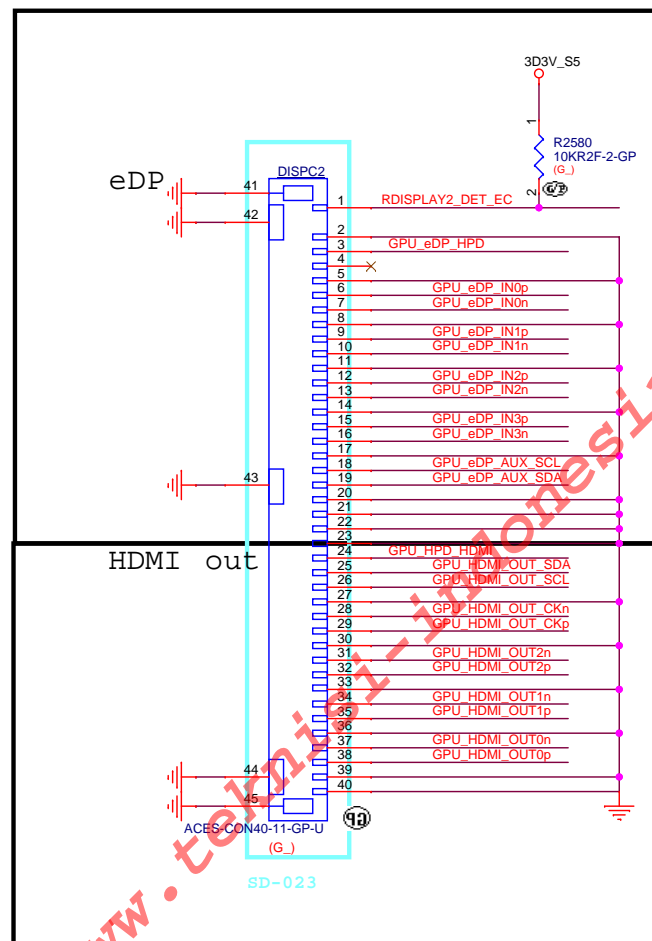
77 GPU_HPD_HDMI << GPU_HPD_HDMI

eDP

86 GPU_eDP_IN0p << GPU_eDP_IN0p
86 GPU_eDP_IN0n << GPU_eDP_IN0n
86 GPU_eDP_IN1p << GPU_eDP_IN1p
86 GPU_eDP_IN1n << GPU_eDP_IN1n
86 GPU_eDP_IN2p << GPU_eDP_IN2p
86 GPU_eDP_IN2n << GPU_eDP_IN2n
86 GPU_eDP_IN3p << GPU_eDP_IN3p
86 GPU_eDP_IN3n << GPU_eDP_IN3n

86 GPU_eDP_AUX_SCL << GPU_eDP_AUX_SCL
86 GPU_eDP_AUX_SDA <<>> GPU_eDP_AUX_SDA

77 GPU_eDP_HPD << GPU_eDP_HPD

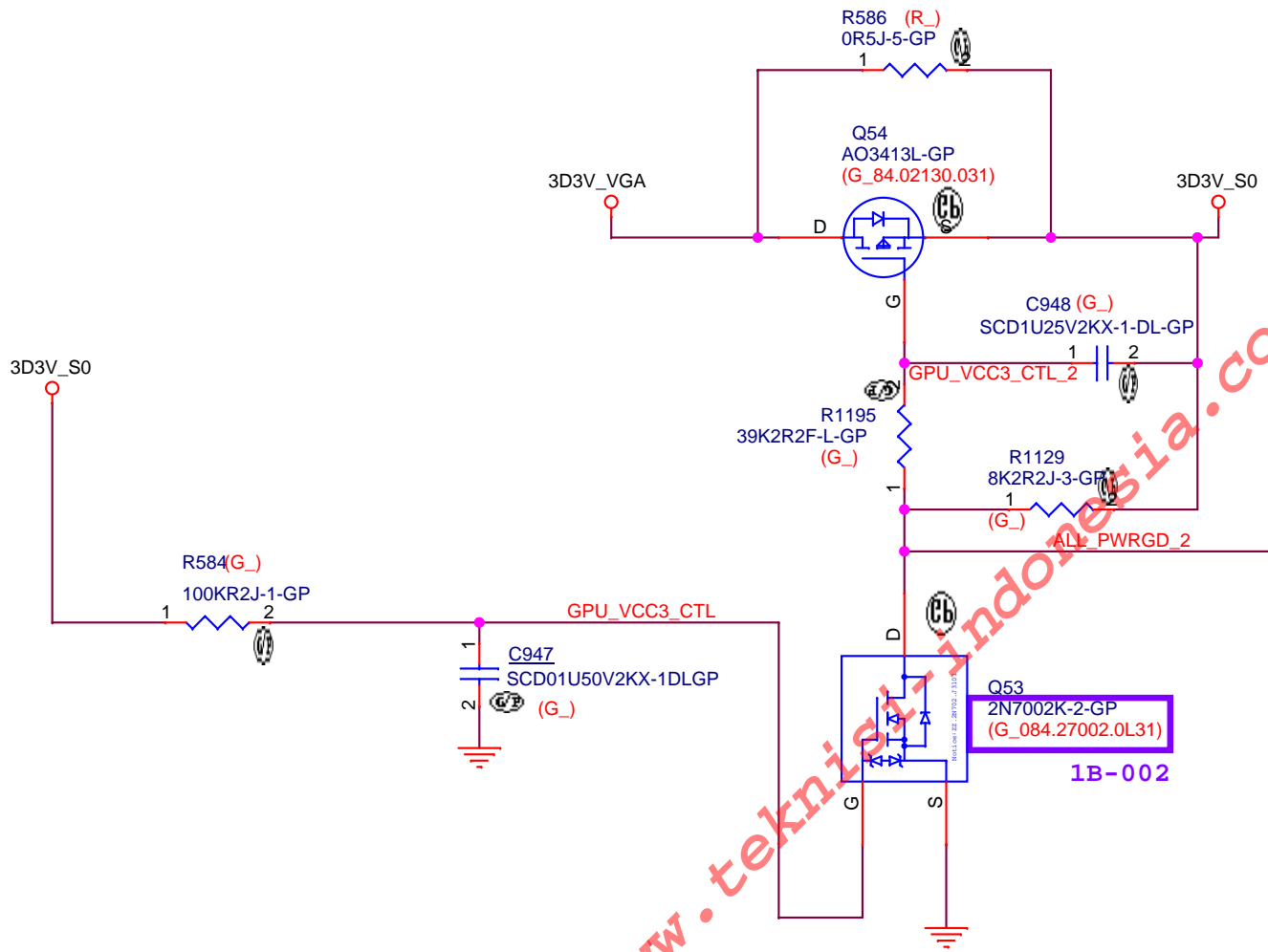


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Title 087_eDP_Repeater_&_IO_port		
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Title

088_HDMI_redriver

Size

A

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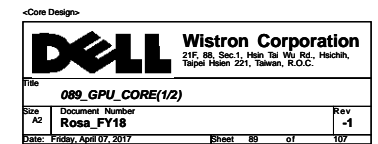
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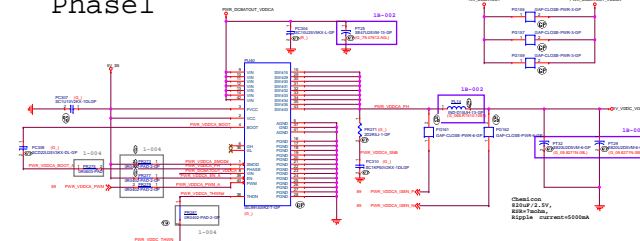
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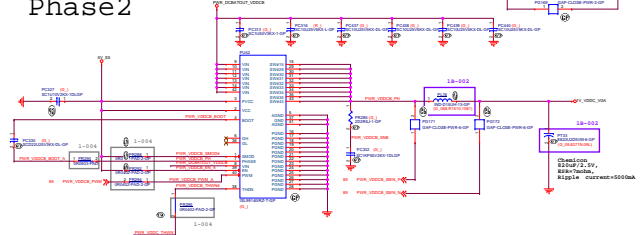


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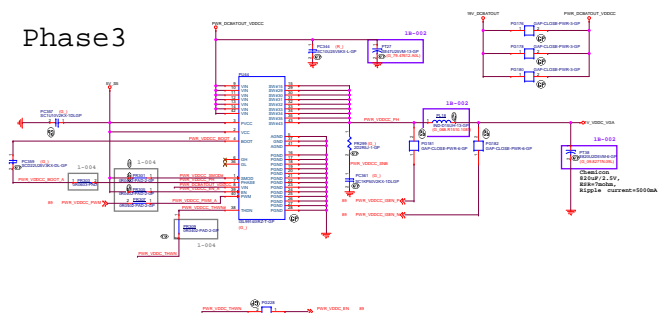
Phase1



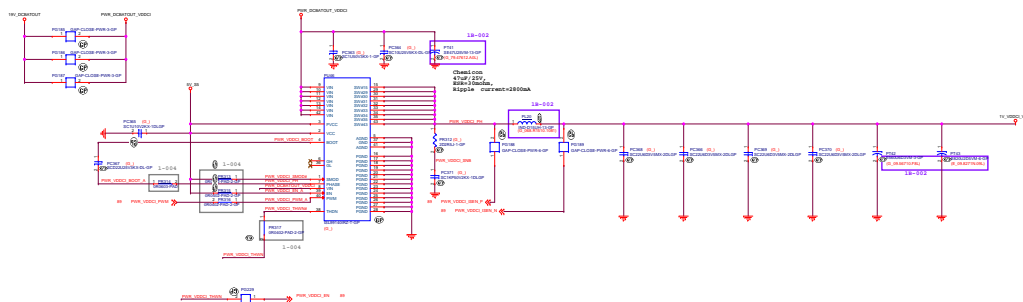
Phase2



Phase3

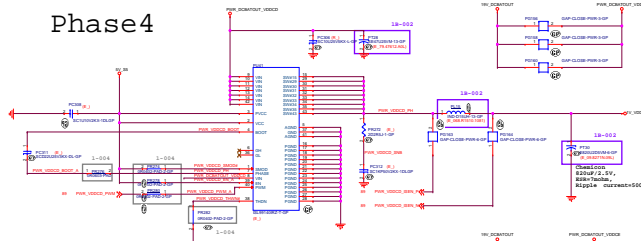


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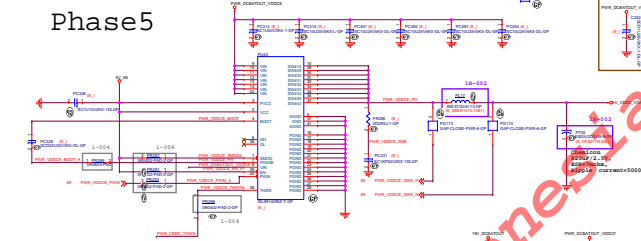


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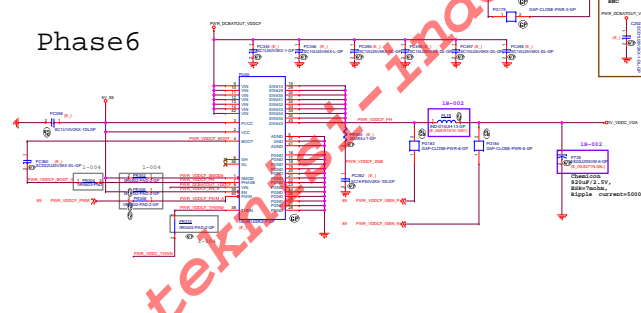
Phase4



Phase5



Phase6



1V_VDDC_VGA

(G_):R16M-G1-80 (50W)

TDC:55A

EDC:105A

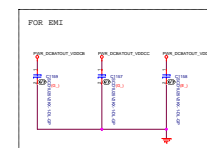
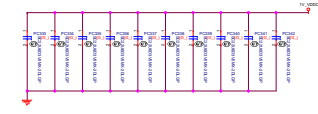
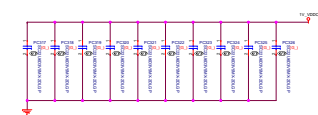
OCp>135A

(E_):R16M-E1 (110W)

TDC:120A

EDC:256A

OCp>270A



1V_VDDCI_VGA

(G_):R16M-G1-80 (50W)

TDC:8A

EDC:12A

OCp>12A

(E_):R16M-E1 (110W)

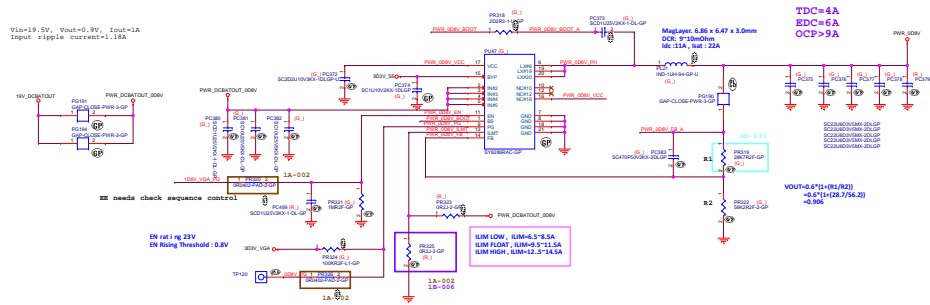
TDC:17A

EDC:25.5A

OCp>38.25A

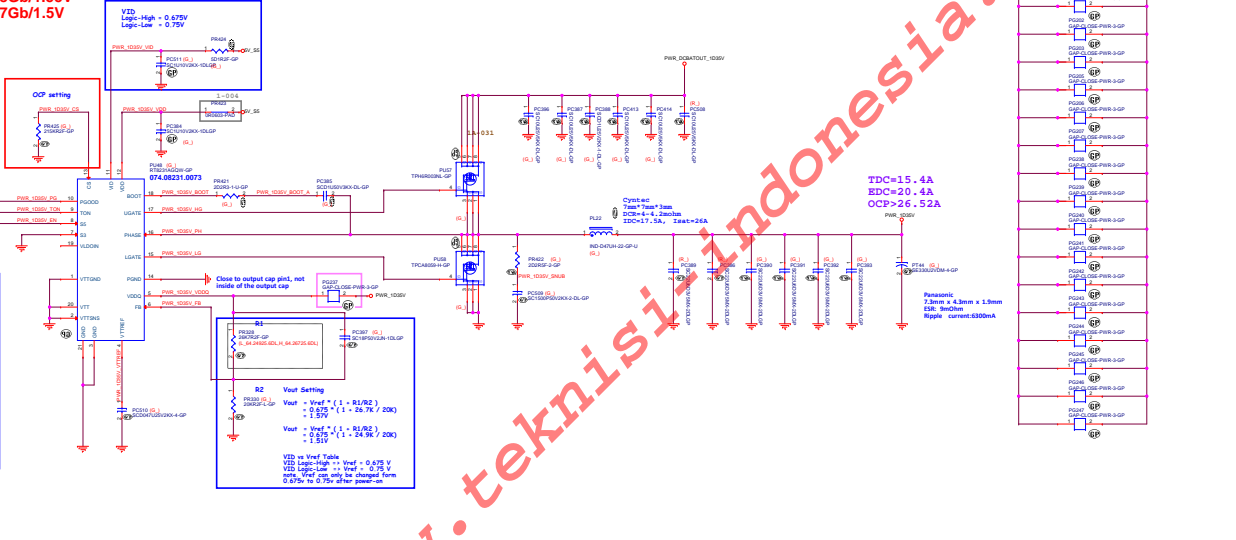
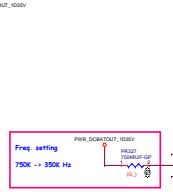
PWR_0D9V

Vin=1.5V, Vout=0.9V, Iout=1A
Input ripple current<1.18A



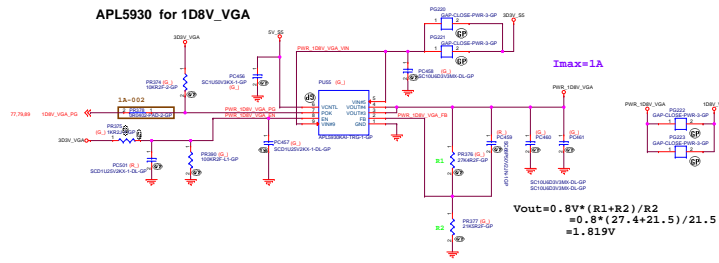
PWR_1D5V

For VRAM
8Gb/1.55V
7Gb/1.5V




PWR_1D8V_VGA_S0

APL5930 for 1D8V_VGA



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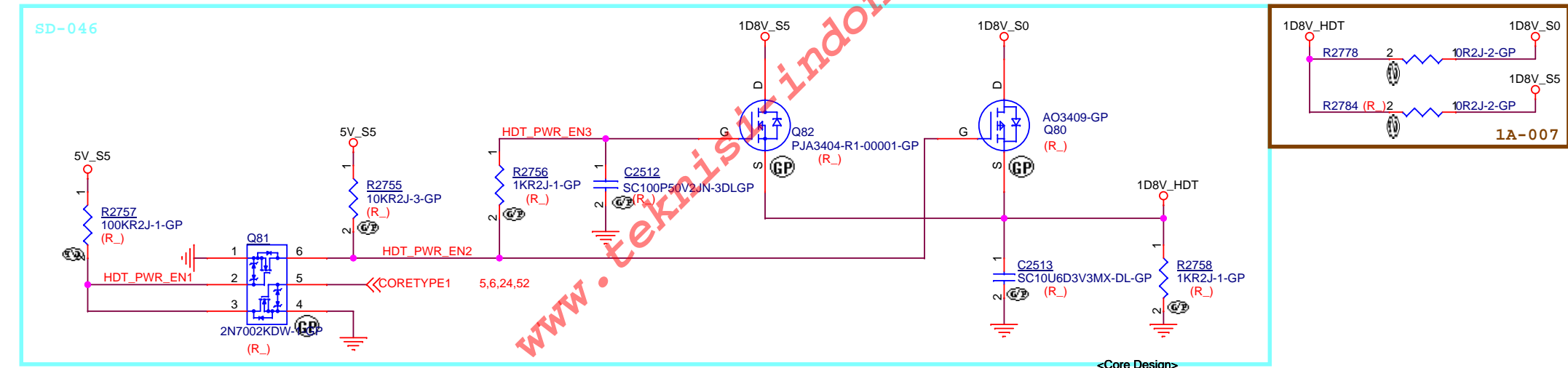
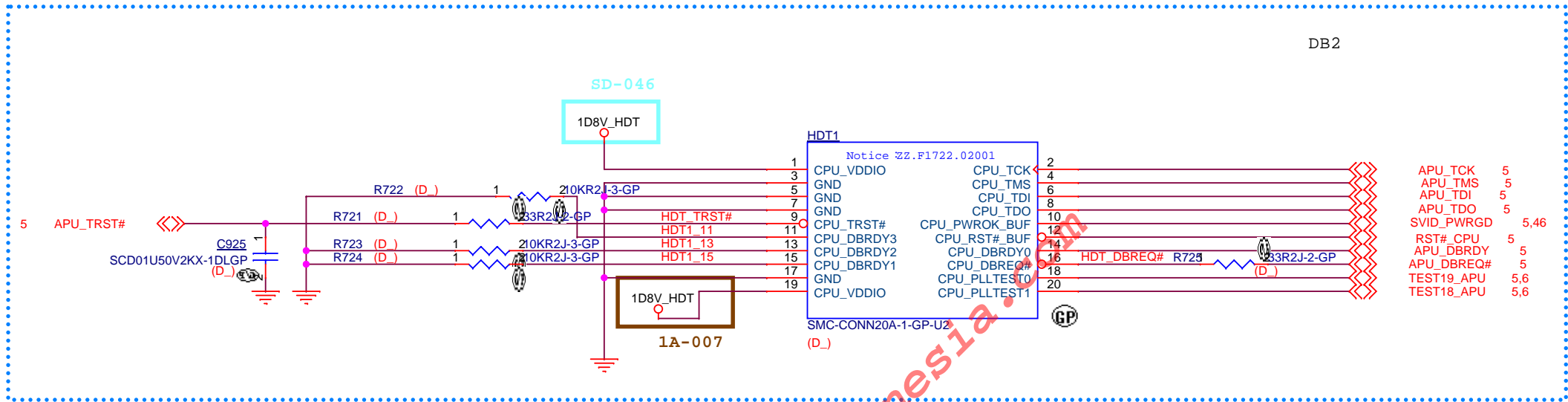
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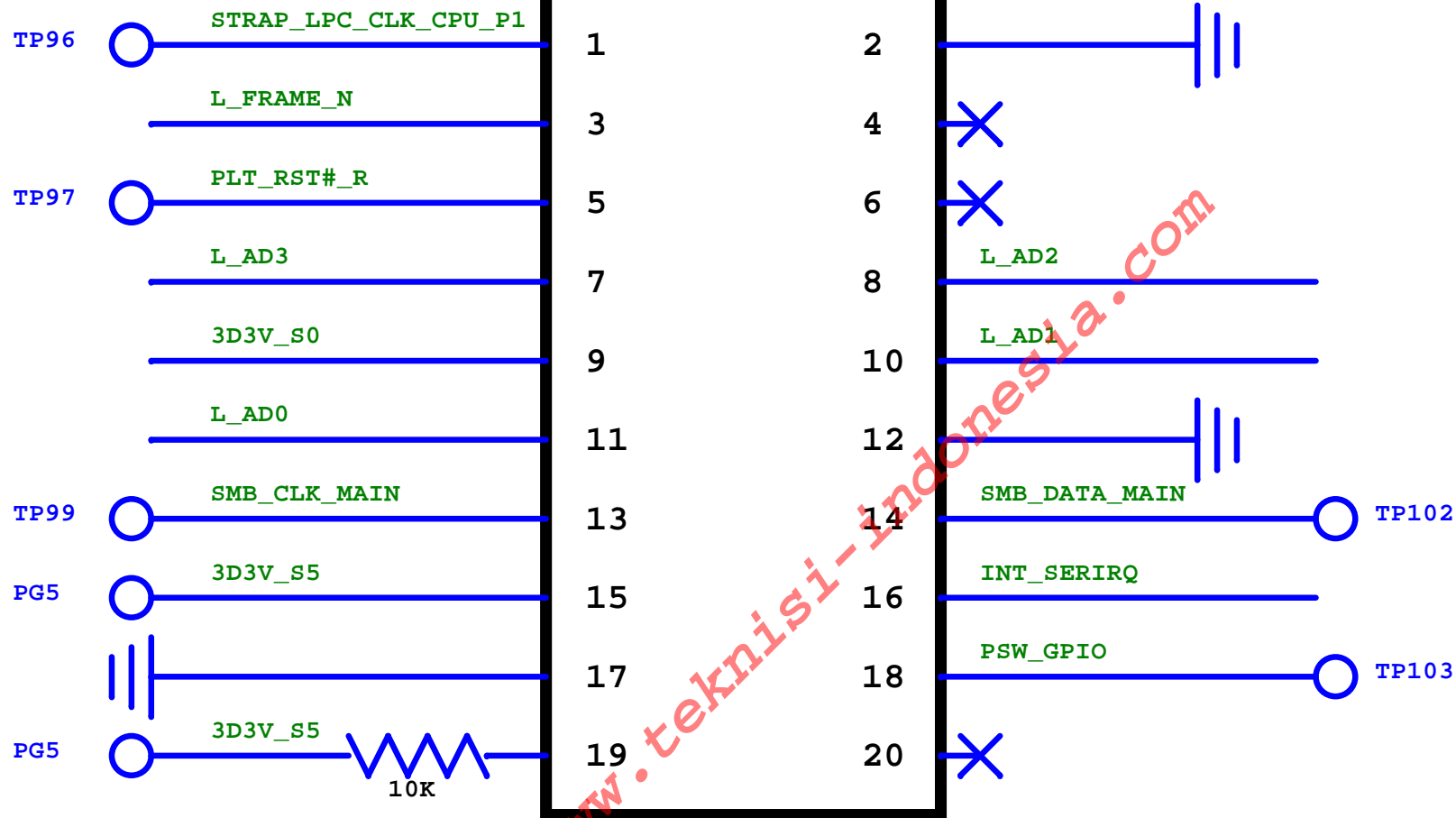
HDT Header



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099_HDT		
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8-1.2-3k(3.33) stack up and impedance

產品編號

8-1.2-3k

注意事項

1. Impedance Control tolerance +/- 10%

完成板厚 (mm)

1.2±0.12

2. Coupon 製作方式及 Impedance report 請依照 Wistron 規範製作

Stack up

L1

TOP

PP

L2

G/P ※ 1

Core

L3

Signal

PP

L4

S/G/P

Core

L5

S/G/P

PP

L6

Signal

Core

L7

G/P

PP

L8

Bottom

Thickness (mil)

1.7

3.0

1.2

4.0

1.2

8.0

1.2

4.0

1.2

8.0

1.2

4.0

1.2

3.0

1.7

88 Ω

85 Ω

82.5 Ω

80 Ω

75 Ω

72 Ω

70 Ω

65 Ω

60 Ω

Impedance Request List

Layer Spec

L1 (Ref. Plane) ※ 1

L3 (Ref. Plane)

L4 (Ref. Plane)

L5 (Ref. Plane)

L6 (Ref. Plane)

L8 (Ref. Plane)

Single Ended Type (Trace width : mil)

33Ω

10.0 (L2)

9.5 (L2/L4); 10.5 (L2/L5)

10.5 (L2/L5)

10.5 (L4/L7)

10.5 (L4/L7); 9.5 (L5/L7)

10.0 (L7)

35Ω

9.0 (L2)

8.5 (L2/L4); 9.5 (L2/L5)

9.5 (L2/L5)

9.5 (L4/L7)

9.5 (L4/L7); 8.5 (L5/L7)

9.0 (L7)

37.5Ω

8.0 (L2)

7.5 (L2/L4); 8.5 (L2/L5)

8.5 (L2/L5)

8.5 (L4/L7)

8.5 (L4/L7); 7.5 (L5/L7)

8.0 (L7)

39Ω

7.5 (L2)

7.0 (L2/L4); 8.0 (L2/L5)

8.0 (L2/L5)

8.0 (L4/L7)

8.0 (L4/L7); 7.0 (L5/L7)

7.5 (L7)

40Ω

7.0 (L2)

6.5 (L2/L4); 7.5 (L2/L5)

7.5 (L2/L5)

7.5 (L4/L7)

7.5 (L4/L7); 6.5 (L5/L7)

7.0 (L7)

45Ω

5.5 (L2)

5.0 (L2/L4); 6 (L2/L5)

6 (L2/L5)

6 (L4/L7)

6 (L4/L7); 5.0 (L5/L7)

5.5 (L7)

48Ω

5.0 (L2)

4.5 (L2/L4); 5.0 (L2/L5)

5.0 (L2/L5)

5.0 (L4/L7)

5.0 (L4/L7); 4.5 (L5/L7)

5.0 (L7)

50Ω

4.5 (L2)

4.0 (L2/L4); 4.5 (L2/L5)

4.5 (L2/L5)

4.5 (L4/L7)

4.5 (L4/L7); 4.0 (L5/L7)

4.5 (L7)

55Ω

3.5 (L2) ※ 2

3.5 (L2/L5) ※ 2

3.5 (L2/L5) ※ 2

3.5 (L4/L7) ※ 2

3.5 (L4/L7) ※ 2

3.5 (L7) ※ 2

Differential Type (Trace width/Space trace/Trace width: mil)

110 Ω

NA

NA

NA

NA

NA

NA

100 Ω

3.5/7/3.5 (L2); 4/10/4 (L2)

3.5/7/3.5 (L2/L5); 4/9/4 (L2/L5)

3.5/7/3.5 (L2/L5); 4/9/4 (L2/L5)

3.5/7/3.5 (L4/L7); 4/9/4 (L4/L7)

3.5/8/3.5 (L5/L7); 4/12/4 (L5/L7)

3.5/7/3.5 (L7); 4/10/4 (L7)

90 Ω

4/5/4 (L2)

4/6/4 (L2/L4); 4/5/4 (L2/L5); 5/7/5 (L2/L5)

4/5/4 (L2/L5); 5/7/5 (L2/L5)

4/5/4 (L4/L7); 5/7/5 (L4/L7)

4/5/4 (L4/L7); 5/7/5 (L4/L7); 4/6/4 (L5/L7)

4/5/4 (L7)

88 Ω

4/4/5/4 (L2)

4/5/4 (L2/L4); 4/4/5/4 (L2/L5)

4/4/5/4 (L2/L5)

4/4/5/4 (L4/L7)

4/5/4 (L5/L7); 4/4/5/4 (L4/L7)

4/4/5/4 (L7)

85 Ω

4/4/4 (L2); 5/6/5 (L2)

4/4/5/4 (L2/L4); 5/6/5 (L2/L4); 4/4/4 (L2/L5); 5/5/5 (L2/L5)

4/4/4 (L2/L5); 5/6/5 (L2/L5) ※ 4

4/4/4 (L4/L7); 5/6/5 (L4/L7) ※ 4

4/4/4 (L4/L7); 5/5/5 (L4/L7); 4/4/5/4 (L5/L7); 5/6/5 (L5/L7)

4/4/4 (L7); 5/6/5 (L7)

82.5 Ω

5/5/5 (L2)

4.5/4.5/4.5 (L2/L4)

5/5/5 (L2/L5)

5/5/5 (L4/L7)

4.5/4.5/4.5 (L5/L7)

5/5/5 (L7)

80 Ω

5/4/5/5 (L2); 6/6/6 (L2)

5/5/5 (L2/L4); 5/5/5/5.5 (L2/L5)

5/5/5/5.5 (L2/L5)

5/5/5/5.5 (L4/L7)

5/5/5/5.5 (L4/L7); 5/5/5 (L5/L7)

5/4/5/5 (L7); 6/6/6 (L7)

75 Ω

6/5/5/6.5 (L2)

6/5/6 (L2/L4); 6/5/5/6.5 (L2/L5)

6/5/5/6.5 (L2/L5)

6/5/5/6.5 (L4/L7)

6/5/6 (L5/L7); 6/5/5/6.5 (L4/L7)

6/5/5/6.5 (L7)

72 Ω

7/5/5/7 (L2)

6/5/5/6.5 (L2/L4); 7/5/7 (L2/L5)

7/5/7 (L2/L5)

7/5/7 (L4/L7)

6/5/5/6.5 (L5/L7); 7/5/7 (L4/L7)

7/5/5/7 (L7)

70 Ω

7/5/7 (L2)

7/5/7 (L2/L4); 7/5/5/7.5 (L2/L5)

7/5/5/7.5 (L2/L5)

7/5/5/7.5 (L4/L7)

7/5/5/7.5 (L4/L7); 7/5/7 (L5/L7)

7/5/7 (L7)

65 Ω

8/5/5/8.5 (L2)

8/5/8 (L2/L4); 8/5/5/8.5 (L2/L5)

8/5/5/8.5 (L2/L5)

8/5/5/8.5 (L4/L7)

8/5/5/8.5 (L4/L7); 8/5/8 (L5/L7)

8/5/5/8.5 (L7)

60 Ω

9/5/5/9.5 (L2)

9/5/5/9.5 (L2/L4); 10/5/10 (L2/L5)

10/5/10 (L2/L5)

10/5/10 (L4/L7)

10/5/10 (L4/L7); 9/5/5/9.5 (L5/L7)

9/5/5/9.5 (L7)

Remark:

※ 1: "Ref. Plane" means the reference plane of the traces.

※ 2: Trace space should be wider than 4.0mil(Wistron internal only).

※ 3: G is GND, P is PWR.

※ 4:update 5/5/5 (L2/L5)8/5/5 (L4/L7) to 5/6/5 (L2/L5)8/5/5 (L4/L7)

Total

44.6

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101_stack up

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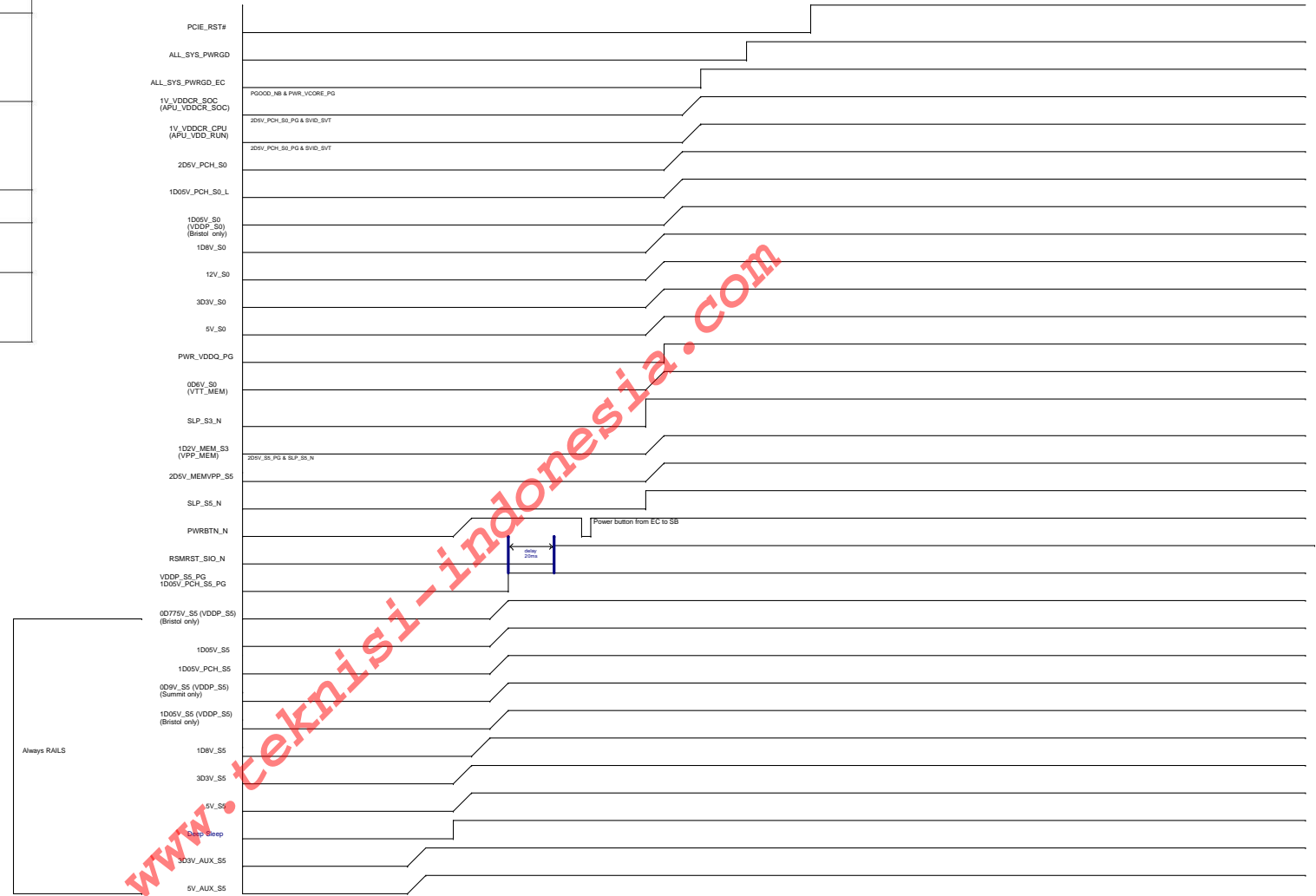
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Table 61. AM4 Power Sequencing Group Definitions with coin cell battery

Group	System Power Domain	Voltages
Group A	G3	VDDBT_RTC_G
Group B	S5	VDD_33_S5, VDD_18_S5, VDDIO_AUDIO, VDDP_S5, VDDCR_SOC_S5
Group C	S3	VDDIO_MEM_S3
	S0	VDD_33, VDD_18, VDDP
Group D	S0	VDDCR_SOC, VDDCR_CPU,



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1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
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102_Power sequence

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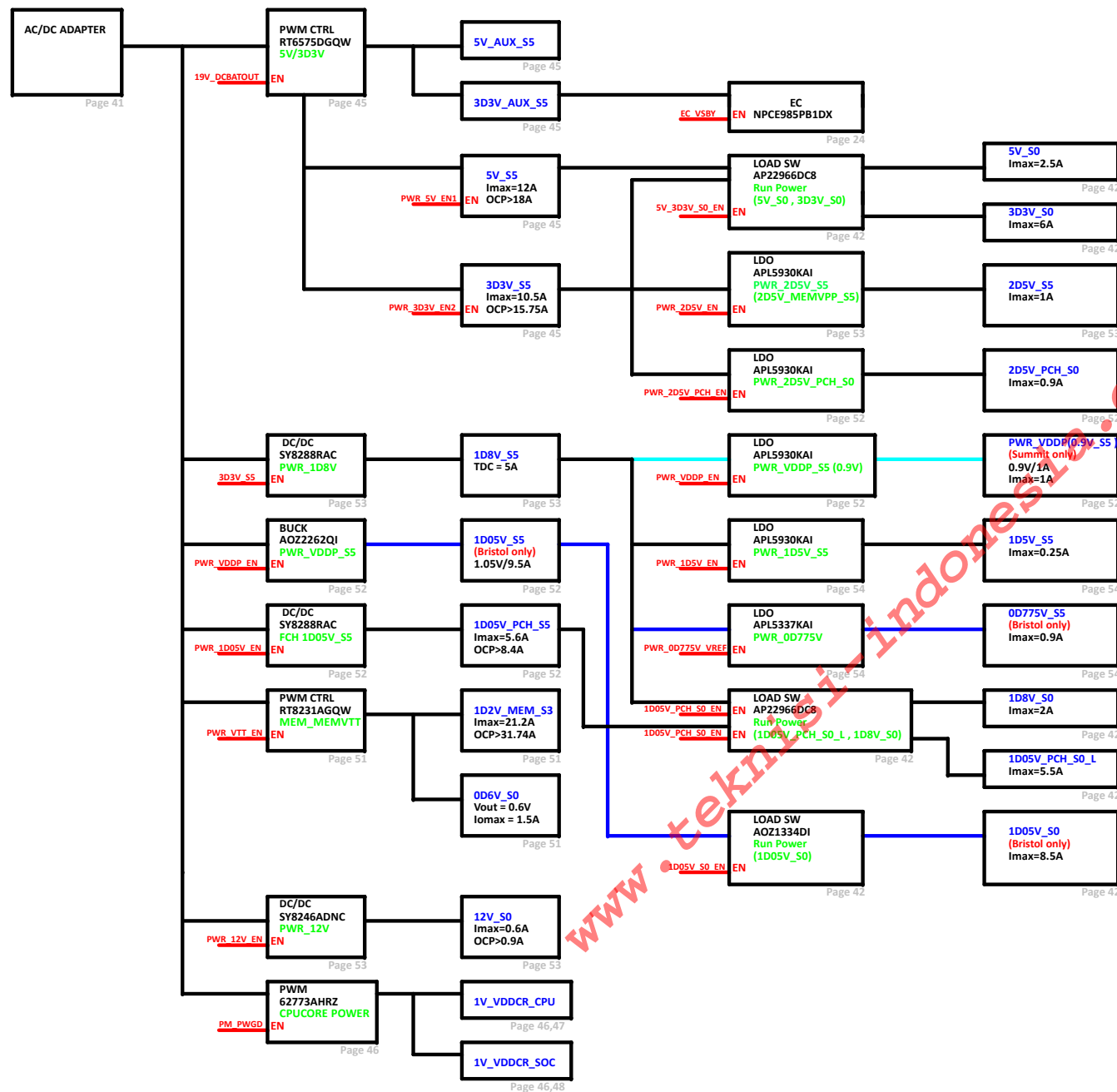
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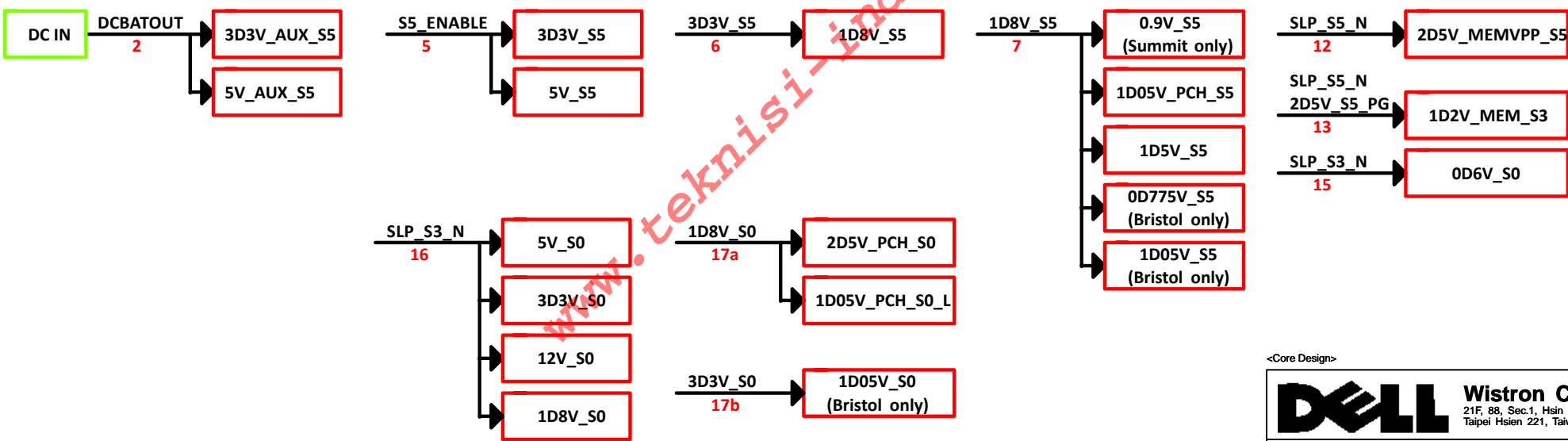
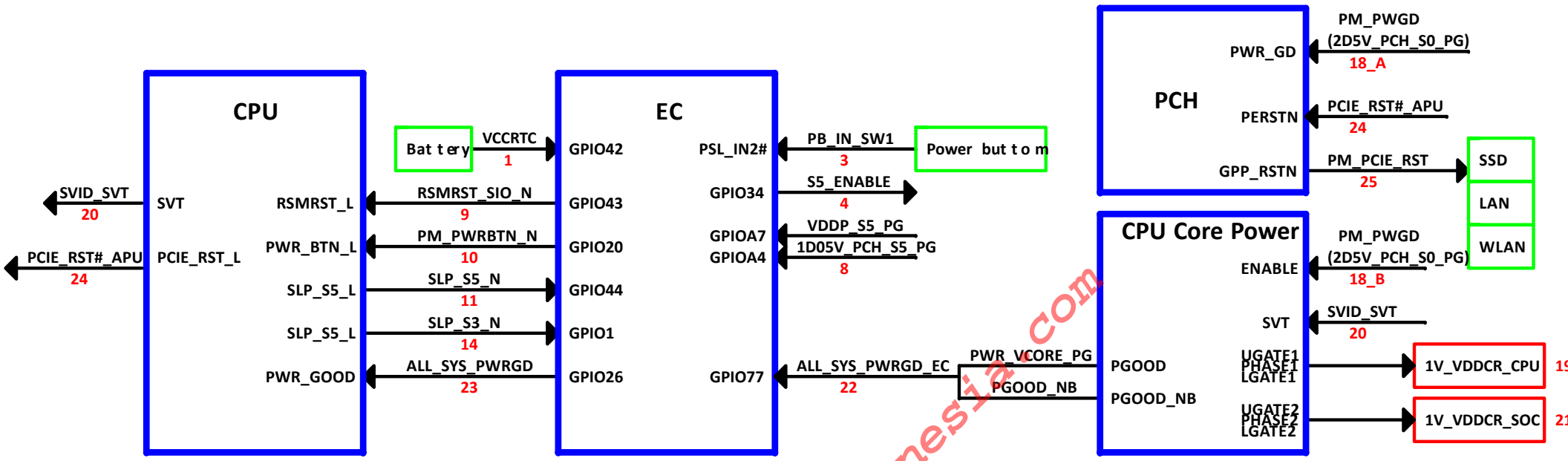


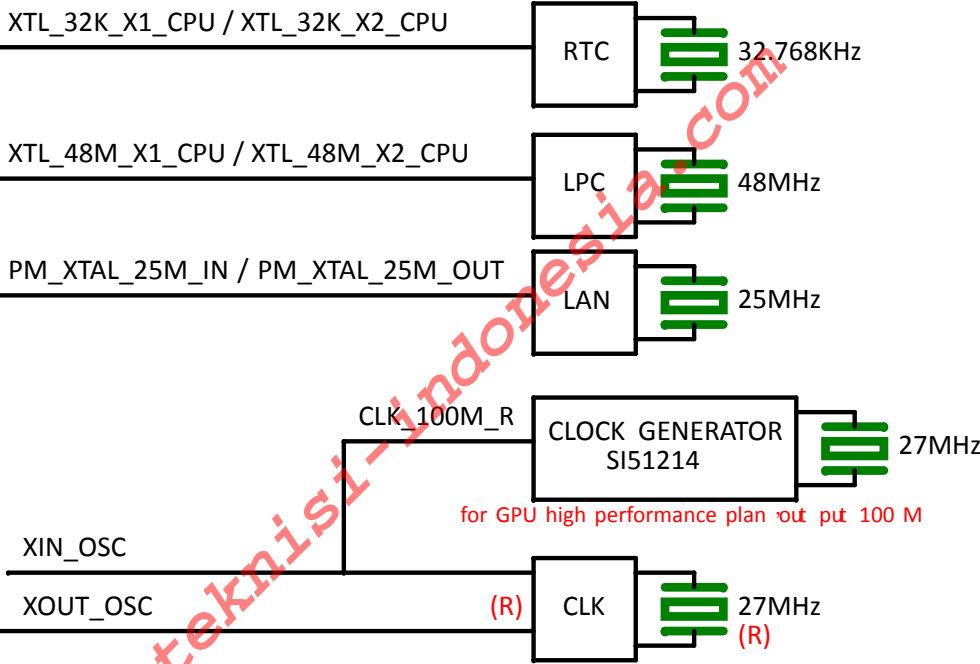
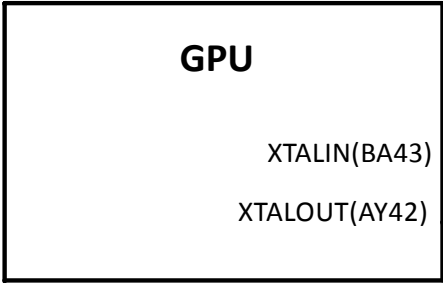
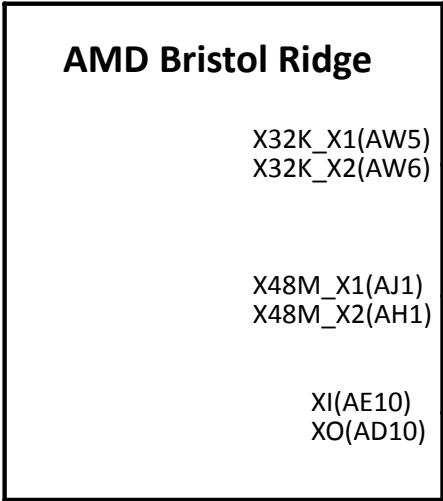
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